BK7239N Datasheet

DS-BK7239N-E07 V1.6

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Contents

1. Features

Wi-Fi®

- IEEE 802.11a/b/g/n/ac/ax 1x1 compliant
- 20 MHz and 40 MHz channel bandwidths for 2.4 GHz and 5 GHz
- Supports 802.11ax with 20 MHz channel up to MCS9
- 2.4 GHz operating frequency range: 2412–2484 MHz
- 5 GHz operating frequency range: 4900–5925 MHz
- Supports downlink Multi-User Multiple-Input Multiple-Output (DL MU-MIMO)
- Supports Orthogonal Frequency Division Multiple Access (OFDMA)
- Supports Target Wake Time (TWT)
- WPA™/WPA2™/WPA3™-Personal support for enhanced security
- Supports STA and SoftAP modes
- Supports concurrent SoftAP + STA
- Integrated Bluetooth/Wi-Fi coexistence (PTA)
- TX power up to +21 dBm
- RX sensitivity -100 dBm

Bluetooth® Low Energy

- Bluetooth Low Energy (LE) 5.4
- Supports Bluetooth Low Energy 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Supported Bluetooth Low Energy features: LE Audio, Angle of Arrival (AoA) and Angle of Departure (AoD) direction finding, 2 Mbps, advertising extensions, and long range
- Supports an antenna array with up to 16 antennas for precise positioning

IEEE 802.15.4

- 2.4 GHz IEEE802.15.4 compliant
- Operating frequency range: 2400–2483.5 MHz
- O-QPSK with 250 kbps data rate

Core

- Arm®v8-M STAR-MC1 MCU at up to 240 MHz:
  - Embedded TrustZone®

  - Supports DSP instructions with SIMD
  - 3.84 CoreMark®/MHz
- UART flash download
- Serial Wire Debug (SWD) interface

Memories

- SiP flash (XIP): 4 MB or none
- SiP PSRAM: 4 MB, 8 MB, or none
- 512 KB Share SRAM
- 64 KB ROM
- eFuse

Security

The BK7239N integrates the IoT Platform Security Suite (IPSS) for cryptograph and system security control. The key features of the IPSS include:

- Secure boot
- Secure debug
- Secure connection
- Firmware Over-The-Air (FOTA)
- Provisioning
- TEE_M
- TrustEngine, which includes the following features:
  - Symmetric schemes, AES-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM (key size 128-bit, 192-bit and 256-bit)
  - Symmetric schemes, SM4-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM
  - Digest schemes, SHA1/224/256
  - Digest scheme, SM3
  - Asymmetric schemes, RSA 1024/2048/3072/4096 and ECCP 192/224/256/384/512/521
  - Asymmetric scheme, SM2
  - Key ladder for key management
  - Lifecycle management
  - True random number generator

Clock Management

- External oscillators: 40 MHz crystal oscillator (XTALH), 32 kHz crystal oscillator (XTALL)
- Internal oscillator: 32 kHz ring oscillator (ROSC)
- 240 MHz/320 MHz/480 MHz PLL (DPLL)

Power Management

- 2.0 to 5.5 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded buck (DC-DC) converter and LDO regulators
- Low power consumption:
  - Active mode RX, 2.4 GHz: 9 mA
  - Active mode RX, 5 GHz: 16 mA
  - Sleep mode: 19 µA
  - Deep sleep mode: 0.7 µA
  - Shutdown mode: 0.2 µA

Peripherals

- GPIOs: 19 in QFN48, 21 in QFN40
- 2x SPI
- 1x QSPI
- 4x UART, 2 with hardware flow control and 1 with flash download support
- 1x SDIO
- 2x I2C
- 1x general-purpose DMA controller (GDMA) with 8 channels
- 1x RGB LED controller
- 12x 32-bit PWM channel
- 1x I2S
- 14-bit AUX ADC, up to 9 channels
- 6x 32-bit general-purpose timer
- 1x watchdog timer
- 1x real-time counter (RTC)
- 1x temperature sensor
- 1x anti-tamper module

Packaging

- QFN48 package, 6 x 6 x 0.75 mm
- QFN40 package, 5 x 5 x 0.75 mm
- Operating temperature range: -40 to +105 °C

Applications

- Home appliance
  - Refrigerator
  - Air conditioner
  - Thermostat
  - Washing machine
  - Robot cleaner
- Smart plug
- Smart lighting
  - Light bulb
  - Light switch
  - Ceiling light
  - Stand light
- Others
  - Remote controller
  - Toy
  - Drone
  - Industrial terminal
  - Factory automation sensor/switch
  - Smart meter
  - Payment terminal
  - Industrial computer
  - Medical devices
  - Kitchen appliances
  - Home automation switch/sensor
  - Door lock
  - Door camera

2. Overview

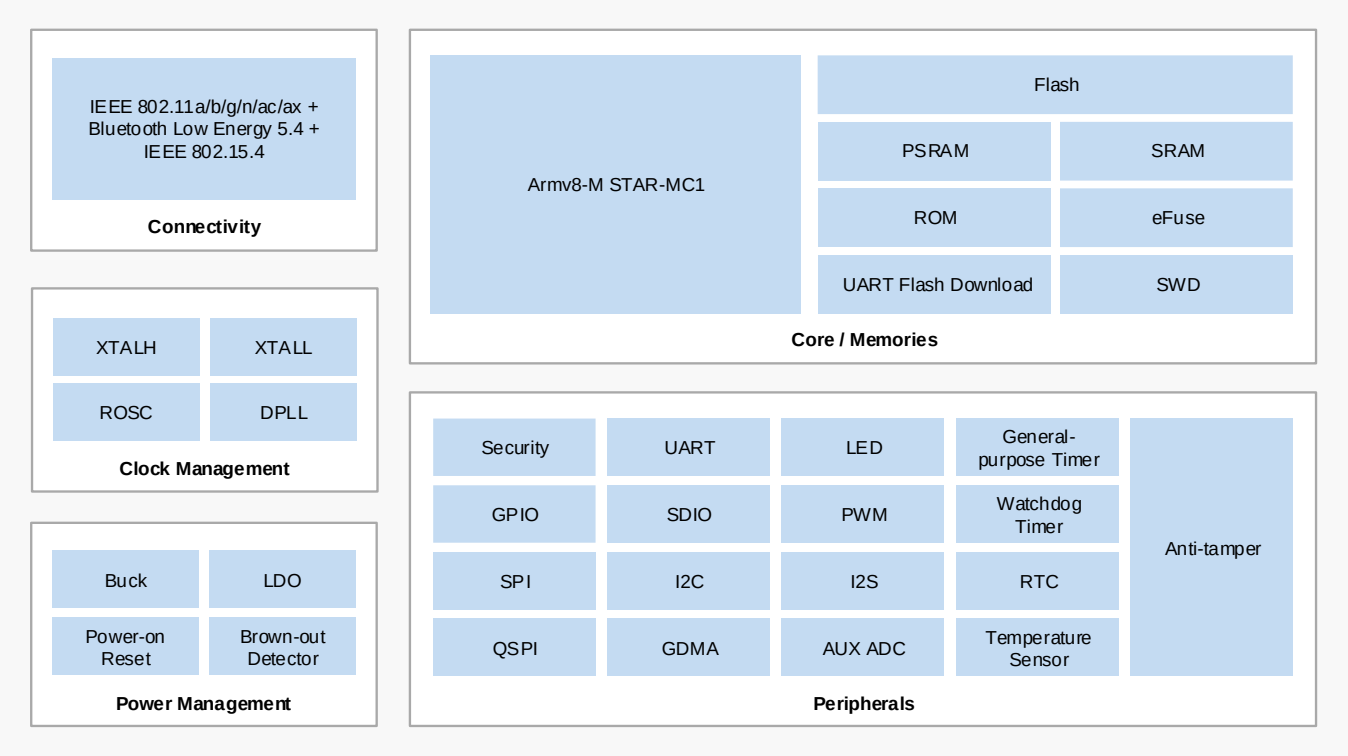
The BK7239N is a highly integrated 1x1 dual-band 2.4/5 GHz Wi-Fi 6 (802.11a/b/g/n/ac/ax), Bluetooth Low Energy (LE) 5.4, and IEEE 802.15.4 multi-protocol connectivity solution designed for applications that require high security and abundant resources. The integration of a 32-bit Armv8-M STAR-MC1 MCU and a comprehensive set of peripherals makes the BK7239N ideal for advanced Internet of Things (IoT) applications.

The BK7239N provides state-of-the-art security based on a powerful security architecture. The BK7239N integrates an IoT Platform Security Suite (IPSS) for cryptograph and system security control. The IPSS embeds all-round and robust security features to set up a top-secret execution environment for IoT devices.

Using advanced design techniques and ultra-low power process technology, the BK7239N delivers high integration, efficient security, and minimal power consumption for a wide range of advanced IoT applications.

Figure 2-1 shows the general block diagram of the BK7239N.

Figure 2-1 BK7239N Block Diagram



The BK7239N devices are offered in two packages. The set of included peripherals varies depending on the package. Table 2-1 shows the list of peripherals available on each package.

Table 2-1 Device Options and Features

Feature		QFN48	QFN40
SiP flash		-	4 MB
SiP PSRAM		8 MB	-
GPIO		19	21
SPI	Master/Slave	2	2
QSPI		1	1
UART		4	4
SDIO		1	1
I2C	Master/Slave	2	2
GDMA		1	1
RGB LED controller		1	1
PWM	PWM0–11	12	12
I2S	Master/Slave	1	1
AUX ADC	14 bits	1	1
	Number of channels	7	9
General-purpose timer		6	6
Watchdog timer		1	1
Real-time counter (RTC)		1	1
Temperature sensor		1	1
Anti-tamper module		1	1
Package		6 x 6 x 0.75 mm QFN48	5 x 5 x 0.75 mm QFN40
Operating voltage		2.0 to 5.5 V	
Operating temperature		-40 to +105 °C	

3. Pin Descriptions

The BK7239N provides Wi-Fi, Bluetooth LE, and IEEE 802.15.4 functionality in two packages of 40 pins and 48 pins.

3.1 QFN48 Pin Descriptions

Figure 3-1 shows the pin assignments of the 6 x 6 mm, 48-pin QFN package.

Figure 3-1 QFN48 Pin Assignments

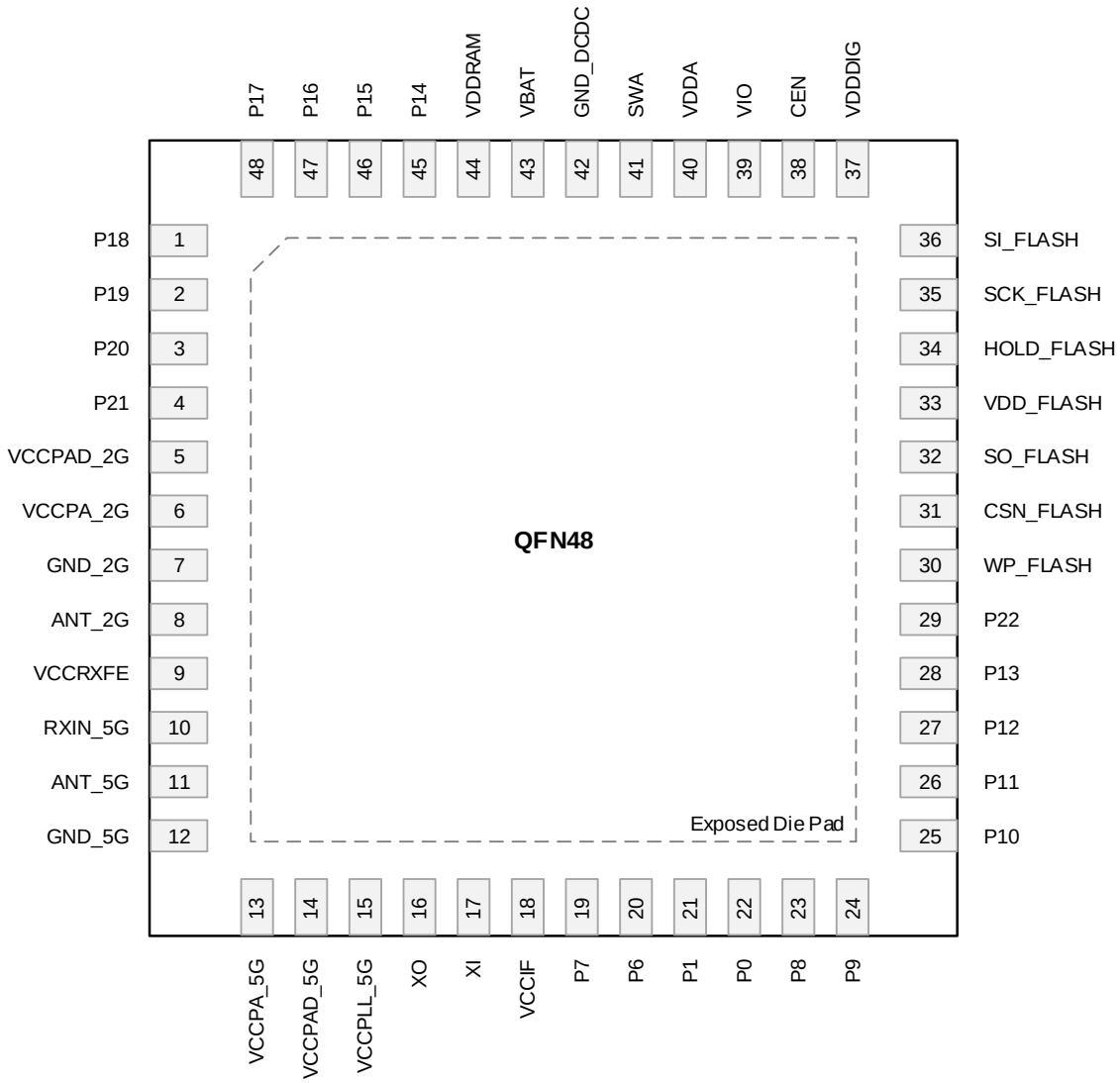


Table 3-1 shows the pin descriptions of the QFN48 package.

Table 3-1 QFN48 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	P18	I/O	Digital	GPIO18: general-purpose I/O
2	P19	I/O	Digital	GPIO19: general-purpose I/O
3	P20	I/O	Digital	GPIO20: general-purpose I/O
4	P21	I/O	Digital	GPIO21: general-purpose I/O
5	VCCPAD_2G	-	Analog input	2.4 GHz RF PA driver power supply
6	VCCPA_2G	-	Analog input	2.4 GHz RF PA power supply
7	GND_2G	-	GND	Ground
8	ANT_2G	-	RF	2.4 GHz RF signal port
9	VCCRXFE	-	Analog input	RF receiver power supply
10	RXIN_5G	-	RF/GND	5 GHz RX input signal port When an external FEM is not present, this pin must be grounded.
11	ANT_5G	-	RF	5 GHz RF signal port
12	GND_5G	-	GND	Ground
13	VCCPA_5G	-	Analog input	5 GHz RF PA power supply
14	VCCPAD_5G	-	Analog input	5 GHz RF PA driver power supply
15	VCCPLL_5G	-	Analog input	5 GHz RF PLL power supply
16	XO	-	Analog output	40 MHz crystal output
17	XI	-	Analog input	40 MHz crystal input
18	VCCIF	-	Analog input	IF power supply
19	P7	I/O	Digital/Analog	• GPIO7: general-purpose I/O • ADC6: analog input channel
20	P6	I/O	Digital/Analog	• GPIO6: general-purpose I/O • ADC5: analog input channel
21	P1	I/O	Digital/Analog	• GPIO1: general-purpose I/O • ADC13: analog input channel
22	P0	I/O	Digital/Analog	• GPIO0: general-purpose I/O • ADC12: analog input channel

Pin #	Name	I/O	Type	Description
23	P8	I/O	Digital/Analog	• GPIO8: general-purpose I/O • ADC10: analog input channel • 32K_XO: 32.768 kHz crystal output
24	P9	I/O	Digital/Analog	• GPIO9: general-purpose I/O • 32K_XI: 32.768 kHz crystal input
25	P10	I/O	Digital	• GPIO10: general-purpose I/O • DL_UART_RX: UART flash download receive data input
26	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX: UART flash download transmit data output
27	P12	I/O	Digital/Analog	• GPIO12: general-purpose I/O • ADC14: analog input channel
28	P13	I/O	Digital/Analog	• GPIO13: general-purpose I/O • ADC15: analog input channel
29	P22	I/O	Digital	GPIO22: general-purpose I/O
30	WP_FLASH	-	Digital output	External flash write protect input
31	CSN_FLASH	-	Digital output	External flash chip select
32	SO_FLASH	-	Digital input	External flash data output
33	VDD_FLASH	-	Analog output	External flash power supply
34	HOLD_FLASH	-	Digital output	External flash hold input
35	SCK_FLASH	-	Digital output	External flash clock input
36	SI_FLASH	-	Digital output	External flash data input
37	VDDDIG	-	Analog output	Digital core LDO output
38	CEN	-	Analog input	Chip enable, active high
39	VIO	-	Analog output	IO LDO output
40	VDDA	-	Analog output	Analog buck/LDO output
41	SWA	-	Analog output	Analog buck switch output
42	GND_DCDC	-	GND	Buck ground
43	VBAT	-	Power	Chip power supply

Pin #	Name	I/O	Type	Description
44	VDDRAM	-	Analog output	EXMEM LDO output
45	P14	I/O	Digital	GPIO14: general-purpose I/O
46	P15	I/O	Digital	GPIO15: general-purpose I/O
47	P16	I/O	Digital	GPIO16: general-purpose I/O
48	P17	I/O	Digital	GPIO17: general-purpose I/O
Die pad	GND_SLUG	-	GND	Ground

3.2 QFN40 Pin Descriptions

Figure 3-2 shows the pin assignments of the 5 x 5 mm, 40-pin QFN package.

Figure 3-2 QFN40 Pin Assignments

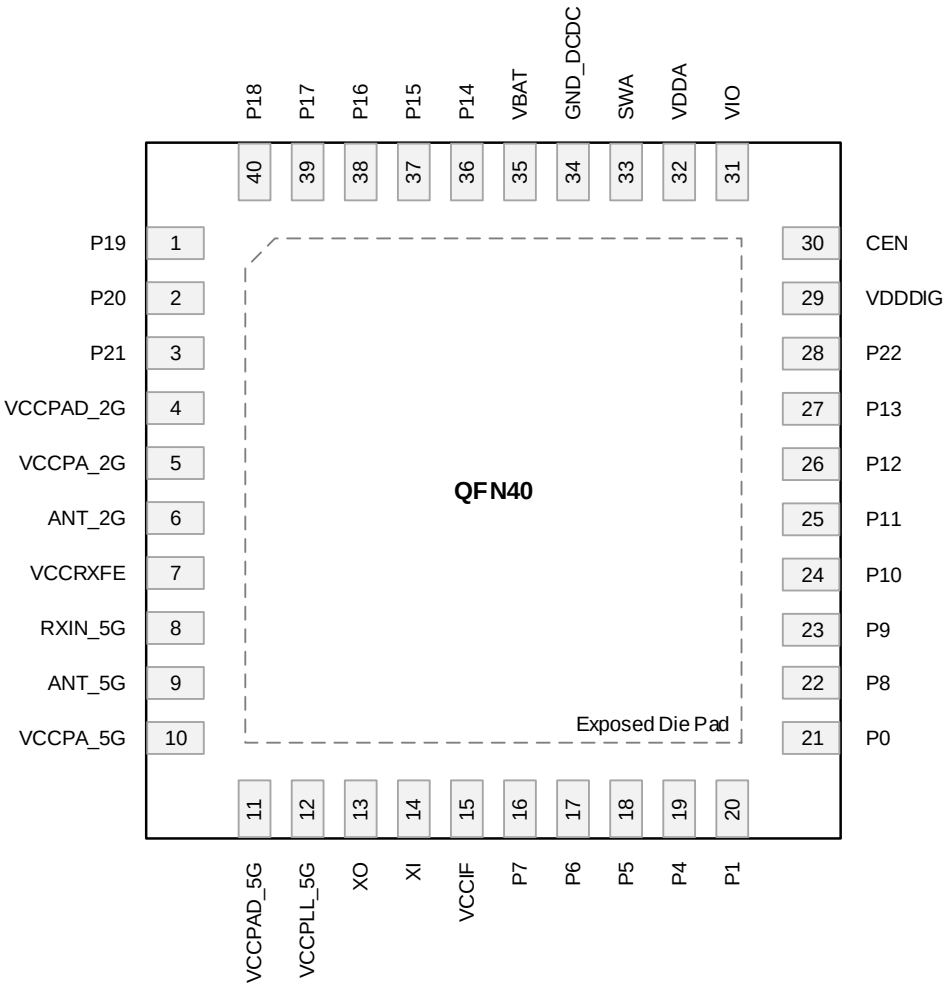


Table 3-2 shows the pin descriptions of the QFN40 package.

Table 3-2 QFN40 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	P19	I/O	Digital	GPIO19: general-purpose I/O
2	P20	I/O	Digital	GPIO20: general-purpose I/O
3	P21	I/O	Digital	GPIO21: general-purpose I/O
4	VCCPAD_2G	-	Analog input	2.4 GHz RF PA driver power supply
5	VCCPA_2G	-	Analog input	2.4 GHz RF PA power supply
6	ANT_2G	-	RF	2.4 GHz RF signal port
7	VCCRXFE	-	Analog input	RF receiver power supply
8	RXIN_5G	-	RF/GND	5 GHz RX input signal port When an external FEM is not present, this pin must be grounded.
9	ANT_5G	-	RF	5 GHz RF signal port
10	VCCPA_5G	-	Analog input	5 GHz RF PA power supply
11	VCCPAD_5G	-	Analog input	5 GHz RF PA driver power supply
12	VCCPLL_5G	-	Analog input	5 GHz RF PLL power supply
13	XO	-	Analog output	40 MHz crystal output
14	XI	-	Analog input	40 MHz crystal input
15	VCCIF	-	Analog input	IF power supply
16	P7	I/O	Digital/Analog	• GPIO7: general-purpose I/O • ADC6: analog input channel
17	P6	I/O	Digital/Analog	• GPIO6: general-purpose I/O • ADC5: analog input channel
18	P5	I/O	Digital/Analog	• GPIO5: general-purpose I/O • ADC4: analog input channel
19	P4	I/O	Digital/Analog	• GPIO4: general-purpose I/O • ADC3: analog input channel
20	P1	I/O	Digital/Analog	• GPIO1: general-purpose I/O • ADC13: analog input channel

Pin #	Name	I/O	Type	Description
21	P0	I/O	Digital/Analog	• GPIO0: general-purpose I/O • ADC12: analog input channel
22	P8	I/O	Digital/Analog	• GPIO8: general-purpose I/O • ADC10: analog input channel • 32K_XO: 32.768 kHz crystal output
23	P9	I/O	Digital/Analog	• GPIO9: general-purpose I/O • 32K_XI: 32.768 kHz crystal input
24	P10	I/O	Digital	• GPIO10: general-purpose I/O • DL_UART_RX: UART flash download receive data input
25	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX: UART flash download transmit data output
26	P12	I/O	Digital/Analog	• GPIO12: general-purpose I/O • ADC14: analog input channel
27	P13	I/O	Digital/Analog	• GPIO13: general-purpose I/O • ADC15: analog input channel
28	P22	I/O	Digital	GPIO22: general-purpose I/O
29	VDDDIG	-	Analog output	Digital core LDO output
30	CEN	-	Analog input	Chip enable, active high
31	VIO	-	Analog output	IO LDO output
32	VDDA	-	Analog output	Analog buck/LDO output
33	SWA	-	Analog output	Analog buck switch output
34	GND_DCDC	-	GND	Buck ground
35	VBAT	-	Power	Chip power supply
36	P14	I/O	Digital	GPIO14: general-purpose I/O
37	P15	I/O	Digital	GPIO15: general-purpose I/O
38	P16	I/O	Digital	GPIO16: general-purpose I/O
39	P17	I/O	Digital	GPIO17: general-purpose I/O
40	P18	I/O	Digital	GPIO18: general-purpose I/O

Pin #	Name	I/O	Type	Description
Die pad	GND_SLUG	-	GND	Ground

3.3 Pin Multiplexing

Each I/O pin of the BK7239N can be configured to perform multiple functions: GPIO function, peripheral functions, and analog functions.

The I/O multiplexer provides one configuration register for each I/O pin. Each I/O pin can be configured as a GPIO or an I/O for peripherals through the GPIOx_FUNC_SEL[6:0] field of the configuration register. Table 3-3 shows the I/O matrix.

Table 3-3 I/O Matrix

Function	GPIOx_FUNC_SEL [6:0] Value	I/O Function Name	I/O Type	Description
GPIO	7'd0	GPIO	High impedance	General-purpose I/O
	7'd1	GPIO	Input	General-purpose I/O
	7'd2	GPIO	Output	General-purpose I/O
	7'd3	GPIO	Input/output	General-purpose I/O
PTA	7'd4	BT_ACTIVE	Input	Bluetooth active
	7'd9	BT_PRIOPRITY	Input	Bluetooth priority
	7'd92	WIFI_ACTIVE	Output	Wi-Fi active
AoA/AoD	7'd5	BT_ANT0	Output	Bluetooth antenna select
	7'd6	BT_ANT1	Output	Bluetooth antenna select
	7'd7	BT_ANT2	Output	Bluetooth antenna select
	7'd8	BT_ANT3	Output	Bluetooth antenna select
Clock	7'd10	CLK_AUXS	Output	Clock output derived from XTALH/LPO_CLK /DPLL
	7'd11	CLK_XTAL	Output	40 MHz clock output

Function	GPIOx_FUNC_SEL [6:0] Value	I/O Function Name	I/O Type	Description
	7'd12	CLK_XTAL_DIV	Output	40 MHz clock output (divide by 1/2/4/8)
	7'd40	LPO_CLK	Output	32 kHz clock output
FEM support	7'd29	FEM_LNA_EN	Output	LNA bypass
	7'd93	WIFI_RX_EN	Output	Receive enable
	7'd94	WIFI_TX_EN	Output	Transmit enable
I2C0	7'd30	I2C0_SCL	Input/output	Serial clock
	7'd31	I2C0_SDA	Input/output	Serial data
I2C1	7'd32	I2C1_SCL	Input/output	Serial clock
	7'd33	I2C1_SDA	Input/output	Serial data
I2S	7'd34	I2S_MCLK	Output	Master clock
	7'd35	I2S_DIN	Input	Serial data input
	7'd36	I2S_DOUT	Output	Serial data output
	7'd37	I2S_SCK	Input/output	Serial clock
	7'd38	I2S_SYNC	Input/output	Frame synchronization
LED	7'd39	LED	Output	LED output
PWM	7'd44	PWM0	Input/output	PWM0 channel
	7'd45	PWM1	Input/output	PWM1 channel
	7'd46	PWM2	Input/output	PWM2 channel
	7'd47	PWM3	Input/output	PWM3 channel
	7'd48	PWM4	Input/output	PWM4 channel
	7'd49	PWM5	Input/output	PWM5 channel
	7'd50	PWM6	Input/output	PWM6 channel
	7'd51	PWM7	Input/output	PWM7 channel
	7'd52	PWM8	Input/output	PWM8 channel
	7'd53	PWM9	Input/output	PWM9 channel
	7'd54	PWM10	Input/output	PWM10 channel
	7'd55	PWM11	Input/output	PWM11 channel

Function	GPIOx_FUNC_SEL [6:0] Value	I/O Function Name	I/O Type	Description
QSPI	7'd56	QSPI_CS	Output	Chip select
	7'd57	QSPI_IO0	Input/output	Data
	7'd58	QSPI_IO1	Input/output	Data
	7'd59	QSPI_IO2	Input/output	Data
	7'd60	QSPI_IO3	Input/output	Data
	7'd61	QSPI_SCK	Input/output	Serial clock
SDIO	7'd62	SDIO_CLK	Input/output	Clock
	7'd63	SDIO_CMD	Input/output	Command/response
	7'd64	SDIO_DATA0	Input/output	Data
	7'd65	SDIO_DATA1	Input/output	Data
	7'd66	SDIO_DATA2	Input/output	Data
	7'd67	SDIO_DATA3	Input/output	Data
SPI0	7'd68	SPI0_MISO	Input/output	Master in slave out
	7'd69	SPI0_MOSI	Input/output	Master out slave in
	7'd70	SPI0_CSN	Input/output	Chip select
	7'd71	SPI0_SCK	Input/output	Serial clock
SPI1	7'd72	SPI1_MISO	Input/output	Master in slave out
	7'd73	SPI1_MOSI	Input/output	Master out slave in
	7'd74	SPI1_CSN	Input/output	Chip select
	7'd75	SPI1_SCK	Input/output	Serial clock
SWD	7'd76	SWCLK	Input	Serial wire clock
	7'd77	SWDIO	Input/output	Serial wire data
Anti-tamper	7'd78	TAMP_RX	Input	Receive data input
	7'd79	TAMP_TX	Output	Transmit data output
UART0	7'd80	UART0_CTS	Input	Clear to send
	7'd81	UART0_RTS	Output	Request to send
	7'd82	UART0_RX	Input	Receive data input

Function	GPIOx_FUNC_SEL [6:0] Value	I/O Function Name	I/O Type	Description
	7'd83	UART0_TX	Output	Transmit data output
UART1	7'd84	UART1_RX	Input	Receive data input
	7'd85	UART1_TX	Output	Transmit data output
UART2	7'd86	UART2_RX	Input	Receive data input
	7'd87	UART2_TX	Output	Transmit data output
UART3	7'd88	UART3_CTS	Input	Clear to send
	7'd89	UART3_RTS	Output	Request to send
	7'd90	UART3_RX	Input	Receive data input
	7'd91	UART3_TX	Output	Transmit data output

Table 3-4 shows the I/O pin multiplexing of analog functions.

Table 3-4 I/O Pin Multiplexing of Analog Functions

GPIO	Analog Function	
	Analog1	Analog2
	AUX ADC	XTALL
GPIO0	ADC12	
GPIO1	ADC13	
GPIO4	ADC3	
GPIO5	ADC4	
GPIO6	ADC5	
GPIO7	ADC6	
GPIO8	ADC10	32K_XO
GPIO9		32K_XI
GPIO10		
GPIO11		
GPIO12	ADC14	
GPIO13	ADC15	

GPIO	Analog Function	
	Analog1	Analog2
	AUX ADC	XTALL
GPIO14		
GPIO15		
GPIO16		
GPIO17		
GPIO18		
GPIO19		
GPIO20		
GPIO21		
GPIO22		

4. Functional Description

4.1 IEEE 802.15.4 Overview

The BK7239N implements IEEE 802.15.4 specification and supports multiple PHY and MAC functionalities.

The 802.15.4 PHY supports Energy detection(ED), Link quality indication(LQI), channel selection, clear channel assessment (CCA), and transmitting as well as receiving packets across the physical medium.

The 802.15.4 MAC supports beacon management, channel access, GTS management, frame validation, acknowledged frame delivery, association, and disassociation. In addition, the MAC sublayer provides hooks for implementing application-appropriate security mechanisms.

802.15.4 Personal Area Networks (PANs) are of two kinds, Beacon Enabled (Slotted) and Non-Beacon Enabled (Unslotted).

In Beacon Enabled PAN, channel time is defined by superframe structure. Superframe have an active and inactive portion, bounded by beacon transmission. Active portion is divided into aNumSuperframeSlots (=16) equally spaced slots and composed of a Contention Access Period (CAP) and a Contention Free Period (CFP). Beacon frame is transmitted as part of the first slot in CAP. GTS slots are located within CFP. Beacon transmission and GTS transmission/reception happens at slot boundary. PAN coordinator only transmits beacon frame. Device only need to receive/track beacon frame. Coordinator tracks beacon of its coordinator and transmits beacon frame for its network. MAC Command Frames and Data (not marked by Higher Layer to be transmitted only during GTS) are transmitted during CAP. For transmission during CAP, CSMA-CA channel access mechanism is used. Two types of CSMA-CA algorithm used. For the beacon enabled PAN, slotted version of CSMA-CA. For the non-beacon enabled PAN, un-slotted version of CSMA-CA.

Non-beacon enabled PAN can be viewed as special case of beacon enabled PAN, where Beacon Interval (BI) is infinite, there is no CFP (GTS) and no inactive portion. Entire period is CAP. And during this CAP, un-slotted version of CSMA-CA is used. Device transmits Command Frame or Data to its coordinator during CAP. In beacon enabled PAN, Coordinator informs the availability of Command Frame or Data in its Beacon and devices requests for the Data based on this information. In non-beacon enabled PAN, higher layer will initiate MLME-POLL request for devices to send data request to coordinator and see if the ACK response suggests data available for the device, based on the Frame Pending field.

Higher layer sets up a PAN, by configuring a device as PAN coordinator. Following that for any device to participate in the PAN operation, need to Associate with one of the coordinator in the PAN. Association is applicable in both beacon enabled and non-beacon enabled PAN.

4.2 RF Transceivers

The BK7239N integrates a high-performance 2.4 GHz Wi-Fi/Bluetooth/802.15.4 transceiver and a high-performance 5 GHz Wi-Fi transceiver. Each transceiver incorporates two on-chip baluns. On the receive side, the on-chip balun converts the single-ended (unbalanced) RF signal from the antenna into a differential (balanced) signal and the low noise amplifier (LNA) amplifies the differential signal to achieve a better noise and linearity trade-off. On the transmit side, the power amplifier (PA) amplifies the differential signal and the on-chip balun converts the differential signal to a single-ended signal for feeding the antenna. This enables transmit and receive operations with either only one ANT pin or one ANT pin (transmit output) and one RXIN pin (when using an external FEM) connected to the antenna. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.3 FEM Support

The BK7239N supports the use of an external Front-End Module (FEM). The external FEMs are controlled by three signals WIFI_TX_EN, WIFI_RX_EN, and FEM_LNA_EN.

Table 4-1 FEM Operating Modes

Operating Mode	WIFI_TX_EN	WIFI_RX_EN	FEM_LNA_EN
Transmit mode	1	0	0
Receive mode	0	1	1
LNA bypass mode	0	1	0
	1	1	X
Standby mode	0	0	0
Not supported	All other states		

4.4 Clock Management

The primary clock sources available in the BK7239N are as follows:

- High-frequency clocks
  - 40 MHz crystal oscillator: it outputs clock signal XTALH
  - Digital PLL (DPLL): it generates 240 MHz clock CLK_240M, 320 MHz clock CLK_320M, and 480 MHz clock CLK_480M

- Low-frequency clocks
  - 32 kHz (32.768 kHz) crystal oscillator: it outputs clock signal XTALL
  - 32 kHz internal ring oscillator (ROSC): it outputs clock signal CLK_ROSC

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32 kHz crystal oscillator XTALL
- 32 kHz clock signal derived from XTALH
- 32 kHz internal oscillator ROSC

The BK7239N also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIOs can output the following clock signals:

- CLK_XTAL: high-frequency crystal clock CLK_XTAL, generally 40 MHz
- CLK_XTAL_DIV: clock derived from CLK_XTAL (division factor 1/2/4/8)
- LPO_CLK: LPO_CLK clock
- CLK_AUXS: clock derived from XTALH/LPO_CLK/DPLL
- I2S_MCLK: reference clock for external audio codec, derived from XTALH

4.5 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown mode or deep sleep mode.

Power-on reset and brown-out reset reset the whole chip to its initial state. The watchdog reset's reset scope is configurable and can be configured to reset the whole chip.

Wake-up from shutdown mode triggers the whole system reset, while wake-up from deep sleep mode triggers the reset of digital blocks.

4.6 Power Management

4.6.1 Power Scheme

The power management system on the BK7239N includes a buck converter and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

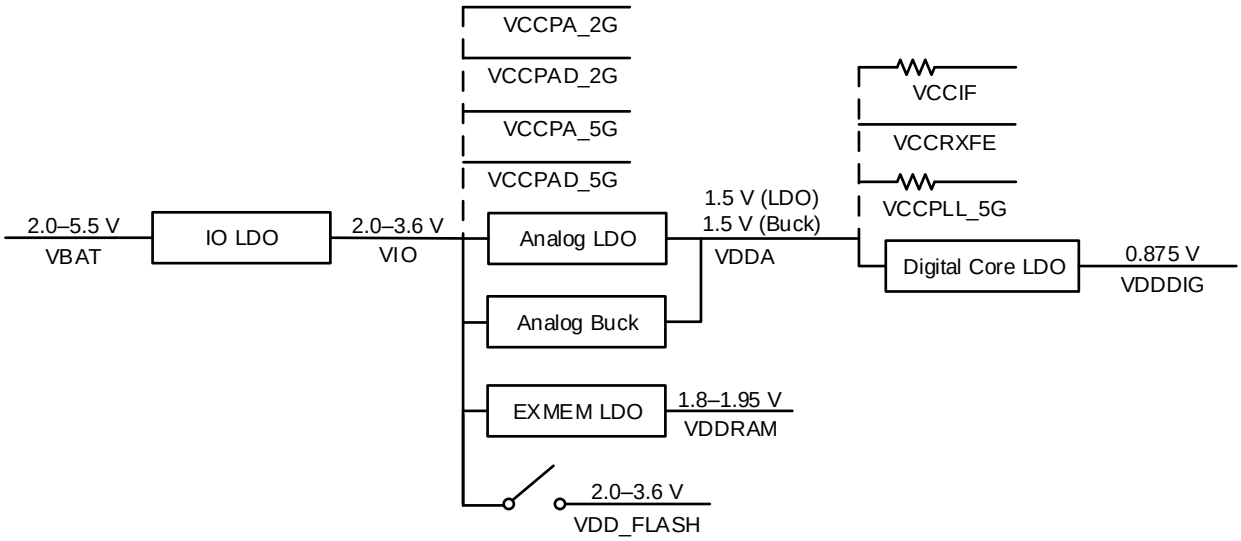
The VBAT is the external main chip supply ranging from 2.0 to 5.5 V. The VBAT generates VIO through the IO LDO regulator. In addition to being the power supply for RF PAs and external flash, the VIO is also the input

supply of analog LDO, analog buck, and EXMEM LDO. The buck and LDOs generate the following main power supplies:

- VDDA: power supply for RF/analog blocks. It is externally connected to VCCIF, VCCRXFE, and VCCPLL_5G to supply power to the RF transceivers, and internally provides power supply to XTAL directly.
- VDDDIG: power supply for digital domain. It provides power supply for the processor, memories, basebands of Wi-Fi, Bluetooth, and 802.15.4, as well as various peripherals.
- VDDRAM: power supply for PSRAM.

Figure 4-1 shows the power distribution of the BK7239N.

Figure 4-1 Internal Power Distribution



Note: Outputs from the buck converter and LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the hardware schematic for details on selecting bypass capacitors.

Figure 4-2 shows the power-up sequence of the BK7239N.

Figure 4-2 BK7239N Power-up Sequence

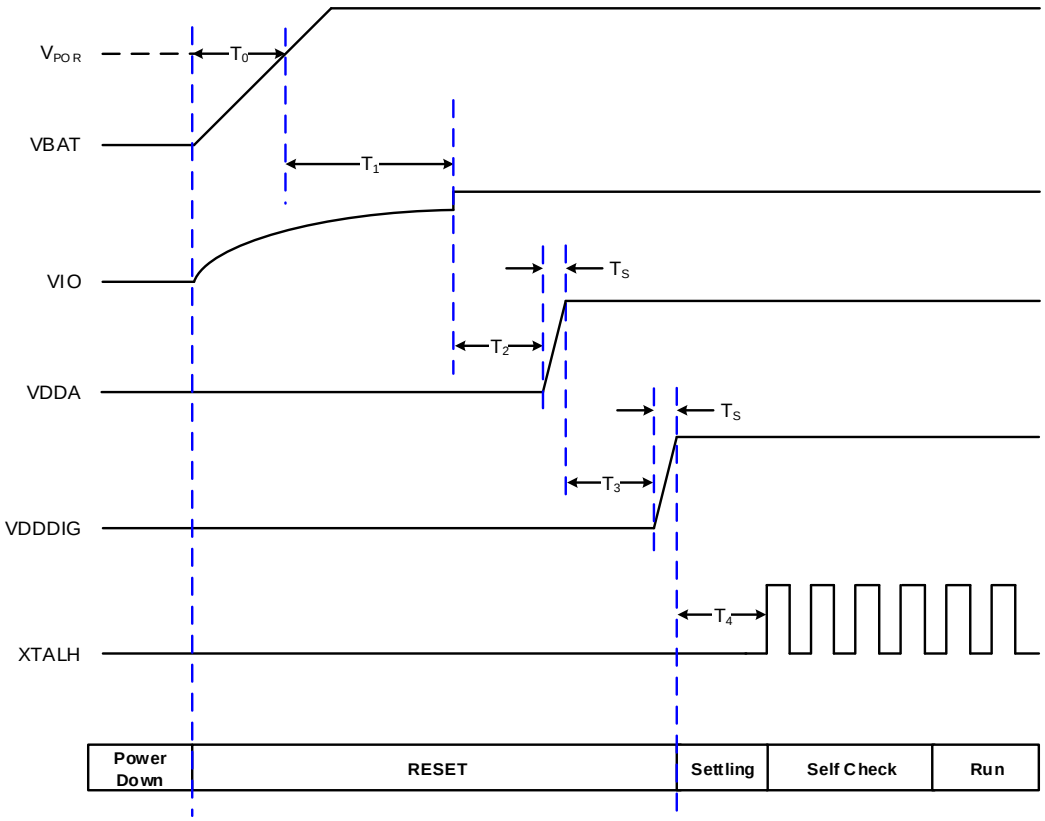


Table 4-2 Timing Parameters of Power-up Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{POR}	VBAT POR threshold	-	1.95	-	V
T_0	VBAT power-up time	200	-	-	μs
T_1	IO LDO ready time	-	2	-	ms
T_2	Analog buck/LDO ready time	-	250	-	μs
T_3	Digital core LDO ready time	-	250	-	μs
T_4	XTALH settle time	100	-	-	μs
T_S	LDO (excl. IO LDO) settle time	0	-	-	μs

Figure 4-3 shows the power-down sequence of the BK7239N.

Figure 4-3 BK7239N Power-down Sequence

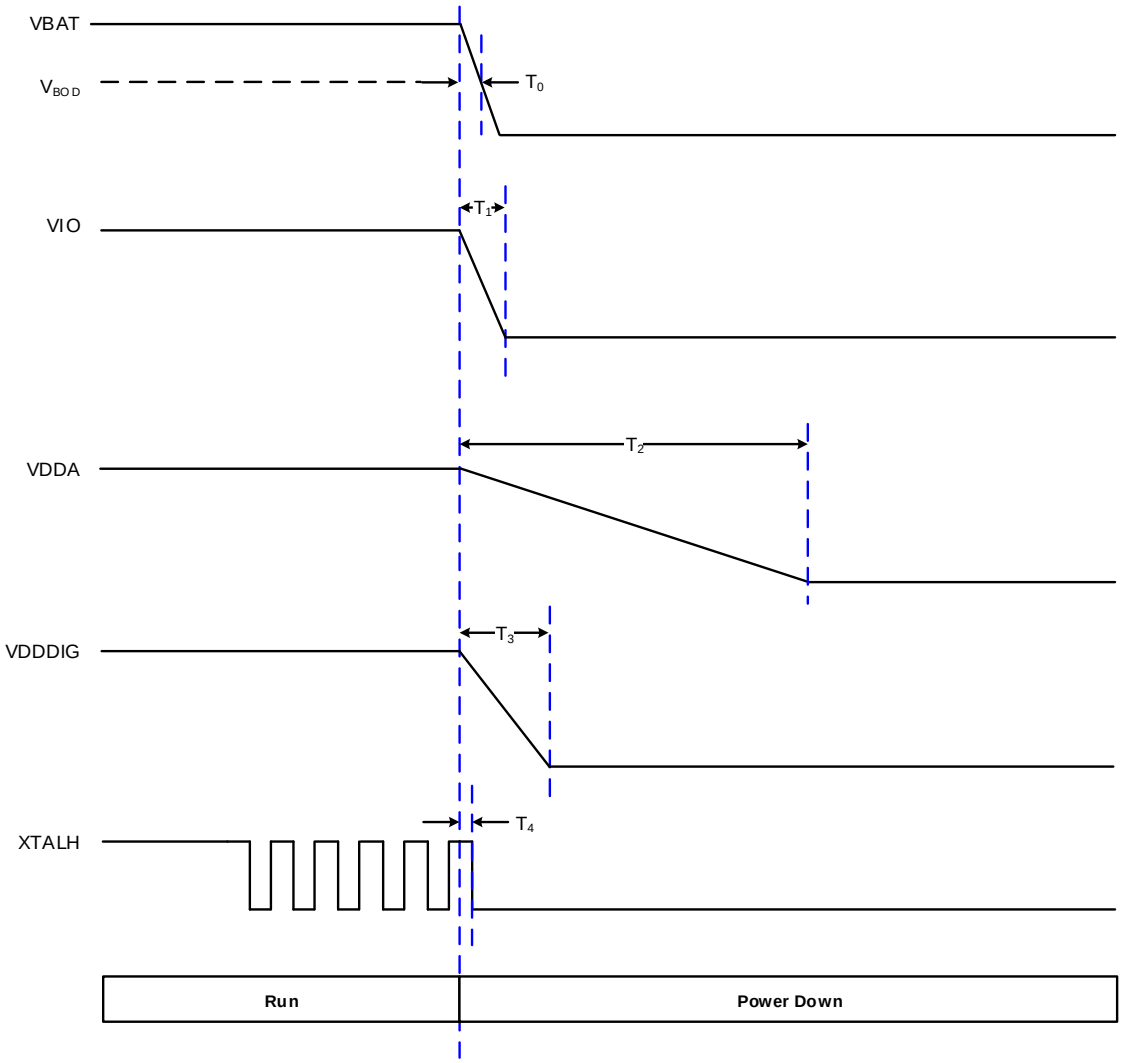


Table 4-3 Timing Parameters of Power-down Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{BOD}	VBAT BOD threshold	-	1.85	-	V
T_0	VBAT power-down time	-	400	-	μs
T_1	IO LDO power-down time	-	600	-	μs
T_2	Analog buck/LDO power-down time	-	400	-	ms
T_3	Digital core LDO power-down time	-	3.5	-	ms
T_4	XTALH power-down time	-	100	-	μs

4.6.2 Power Modes

The BK7239N supports three low-power modes except active mode, namely shutdown mode, deep sleep mode, and sleep mode, among which the shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

Deep Sleep Mode: All circuits are powered down except the AON block. A GPIO event or an RTC event can power up the system again. The retention register holds its content.

Sleep Mode: The MCU and all digital blocks stop their clocks. A GPIO event or an RTC event can bring the system back to active mode.

Active Mode: The MCU is active, and all peripherals are available.

4.7 I/O Multiplexer (IOMUX)

The BK7239N has an I/O multiplexer (IOMUX) that allows the use of I/O pins as either GPIOs or I/Os for peripherals. The I/O multiplexer provides one configuration register for each I/O pin. The GPIOx_FUNC_SEL[6:0] field of the configuration register selects I/O functions:

- When GPIOx_FUNC_SEL[6:0] is set to 0 to 3, the I/O is configured as a GPIO. The GPIO type can be configured as:
  - High impedance
  - Input
  - Output
  - Input/output
- When GPIOx_FUNC_SEL[6:0] is set to 4 to 94, the I/O is configure as an I/O of a peripheral. It's should be noted that multiple I/Os cannot be configured as I/Os of the same peripheral.

The I/O multiplexer provides additional registers that, in GPIO mode, allow for simultaneous querying of the interrupt status and input status of all GPIOs, as well as simultaneous configuration of the output of all GPIOs.

4.8 General-purpose I/Os (GPIO)

The BK7239N has up to 21 GPIOs, which can be configured as high-impedance, input, output, or input/output. All GPIOs are shared with peripheral and/or analog functions.

The main features of GPIOs include:

- Push-pull

- Internal pull-up/down resistors
- Configurable drive strength
- Interrupt generation:
  - High or low level
  - Rising or falling edge

4.9 SPI Interfaces (SPI)

The BK7239N integrates two SPI interfaces that can operate in master or slave mode. The SPI interfaces allow a clock frequency up to 40 MHz in both master and slave modes.

The SPI interfaces support the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Embedded 64-depth RX FIFO and 64-depth TX FIFO with DMA capability

4.10 Quad SPI Interface (QSPI)

The BK7239N embeds a Quad SPI interface that provides support for communicating with external flash, PSRAM, or AMOLED displays. The QSPI interface allows communicating up to 80 MHz.

The features of the QSPI interface are listed below:

- Single, dual, or quad SPI input/output
- Two functional modes: indirect mode and memory-mapped mode
- Fully programmable opcode and frame format
- Integrated RX FIFO and TX FIFO
- Supports 8, 16, and 32-bit data accesses

4.11 UART Interfaces (UART)

The BK7239N includes four Universal Asynchronous Receiver/Transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 10 Mbps.

UART0 supports flash download. When UART0 is used for flash download, UART0_RX and UART0_TX are mapped to GPIO10 as DL_UART_RX and GPIO11 as DL_UART_TX, respectively.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)
- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)
- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Hardware flow control with RTS and CTS signals (UART0 and UART3)
- Flash download (UART0)
- Programmable digital filter

4.12 SDIO Interface (SDIO)

A secure digital input/output (SDIO) host/slave interface is available on the BK7239N. It can be used as a host to read external SD cards or used by an external host as a slave to communicate with chips. The SDIO interface allows a maximum clock speed of 80 MHz.

The SDIO features include the following:

- SD memory card specification version 2.0 compliant
- SDIO card specification version 2.0 compliant
- Two data bus modes: 1-bit mode (default) and 4-bit mode
- Data transfer up to 40 Mbyte/s for the host mode and 20 Mbyte/s for the slave mode
- Supports DMA capability, allowing high-speed transfer without CPU load

4.13 I2C Interfaces (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7239N embeds two I2C interfaces, which can operate in master or slave mode.

The features of the I2C interfaces are listed below:

- Master and slave modes
- Standard-mode (up to 100 kbps)
- Fast-mode (up to 400 kbps)
- Fast-mode Plus (up to 1 Mbps)

- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection
- Embedded 16-byte TX FIFO and 16-byte RX FIFO

4.14 GDMA Controller (GDMA)

The BK7239N has a general-purpose DMA controller (GDMA) with 8 DMA channels to unload CPU activity. The 8 channels are shared by peripherals that have DMA capabilities.

The GDMA controller can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). The GDMA controller allows peripheral to memory, memory to memory, and memory to peripheral, peripheral to peripheral data transfers at a high speed.

The GDMA controller supports channel isolation. The DMA channels can be configured as secure/non-secure and as privileged/unprivileged channels:

- A non-secure channel performs non-secure DMA transfers
- A secure channel can perform secure or non-secure DMA transfers, with
  - Secure or non-secure data read from the source address
  - Secure or non-secure data write to the destination address
  - Via a TrustZone-aware DMA AHB master port
- An unprivileged channel performs unprivileged DMA transfers
- A privileged channel performs privileged DMA transfers

A selection of peripherals on the BK7239N have DMA capabilities, including UART0, UART1, UART2, UART3, SPI0, SPI1, SDIO, and I2S.

4.15 RGB LED Controller (LED)

The BK7239N has a RGB LED controller that supports Return-to-Zero (RZ) communication protocol. With an external LED driver IC, the RGB LED controller can support up to 1024 LED beads. The duty cycle of code 0 and code 1 of RZ communication can be configured by register. The reset signal length is also configurable.

4.16 PWM Module (PWM)

The BK7239N has an advanced-control PWM module (PWM). The PWM module consists of 12 32-bit auto-reload counters driven by 12 programmable prescalers. The PWM module has 12 independent channels for input capture, pulse edge counting, or generation of output waveforms (output compare).

The 12 independent channels can be allocated to any counter comparator output. Each of the 12 channels can generate independent waveforms or complementary waveforms when coupled with any other channels.

The features of the PWM module are listed here:

- 12 32-bit up, down, up-and-down auto-reload counters
- 12 8-bit programmable prescalers capable of dividing the clock frequency of each counter by any factor between 1 and 256
- 12 independent channels for:
  - Input capture
  - Pulse edge counting
  - PWM generation (edge or center-aligned mode)
- Complementary outputs with programmable dead-time and configurable dead-time mode
- Synchronization circuit to control the counter with external signals and to interconnect several counters together
- Repetition counter to update the registers only after a given number of cycles of the counter
- Dedicated hardware support for smooth and precise LED dimming/fading
- Interrupt generation on the following events:
  - Update: counter overflow or underflow, counter initialization (by software or internal/external trigger)
  - Counter start
  - Input capture
  - Output compare
  - LED fading end
- Change of polarity, duty cycle, and base frequency on every PWM period
- Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes

4.17 I2S Interface (I2S)

The BK7239N integrates an I2S interface that supports master and slave modes with a sampling rate from 8 kHz to 384 kHz. The I2S interface supports both PCM mono channel mode and I2S stereo channel mode.

Listed here are the I2S features:

- Master or slave mode
- Full duplex or half-duplex communication
- Various sampling rates
- 12-bit programmable prescaler
- Multiple I2S protocols supported:
  - I2S Philips standard
  - MSB-Justified standard (Left-Justified)
  - LSB-Justified standard (Right-Justified)
  - PCM standard
- Programmable data order with LSB first or MSB first
- Programmable data width between 1 and 32 bits
- Programmable clock polarity
- Integrated 32-bit RX FIFO and 32-bit TX FIFO, both with a depth of 32 x 3 channels
- Master clock can be output to drive external audio devices.

4.18 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 14-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot or continuous mode.

The AUX ADC module has the following features:

- Programmable sampling rates from 51.28 kHz to 1.538 MHz
- 14-bit resolution
- Up to 9 external analog input channels: ADC3/4/5/6/10/12/13/14/15
- Five internal dedicated channels:
  - VBAT monitoring channel (VBAT/4), connected to ADC0
  - Internal temperature sensor (TEMP), connected to ADC7
  - TSSIO, connected to ADC8
  - Internal debug channels, connected to ADC9/11
- Conversion modes:
  - One-shot mode

- Continuous mode

4.19 Timer Groups (TIMG)

The BK7239N includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, division factor between 1 and 16
- The real-time value of the counter can be read.

4.20 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect and recover from failures or malfunctions. The watchdog timer triggers a reset on expiry of a specified time period.

The watchdog timer runs on a 16 kHz clock derived from LPO_CLK (LPO_CLK/2). The division ratio for the 16 kHz clock can be 2, 4, 8, or 16, allowing for a maximum programmable period of up to 65.536 (2^16/1 kHz) seconds.

4.21 Real-time Counter (RTC)

The real-time counter (RTC) module features a 36-bit counter and a tick event generator. The RTC clock source can be selected from XTALL or ROSC. It is used for low-power timing, and it can keep running even when the system is in deep sleep mode.

4.22 Temperature Sensor

The BK7239N integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results can be read from the AUX ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

4.23 Anti-tamper Module

The anti-tamper module is designed to prevent, detect, and respond to physical attacks on the BK7239N chip. Once a tampering attempt is detected, it reports an interrupt to the MCU.

4.24 Security

The BK7239N provides state-of-the-art security based on a powerful security architecture. It integrates a total security solution for Internet of Things (IoT), IoT Platform Security Suite (IPSS). The IPSS aims to set up a top-secret execution environment for IoT devices. With the state-of-the-art security technology, it is intended for power/cost/resource sensitive IoT market applications.

The IPSS introduces a fundamental software IP solution for cryptograph and system security control. The key features of the IPSS include:

- Secure boot
- Secure debug
- Secure connection
- Firmware Over-The-Air (FOTA)
- Provisioning
- TEE_M
- TrustEngine

System Architecture

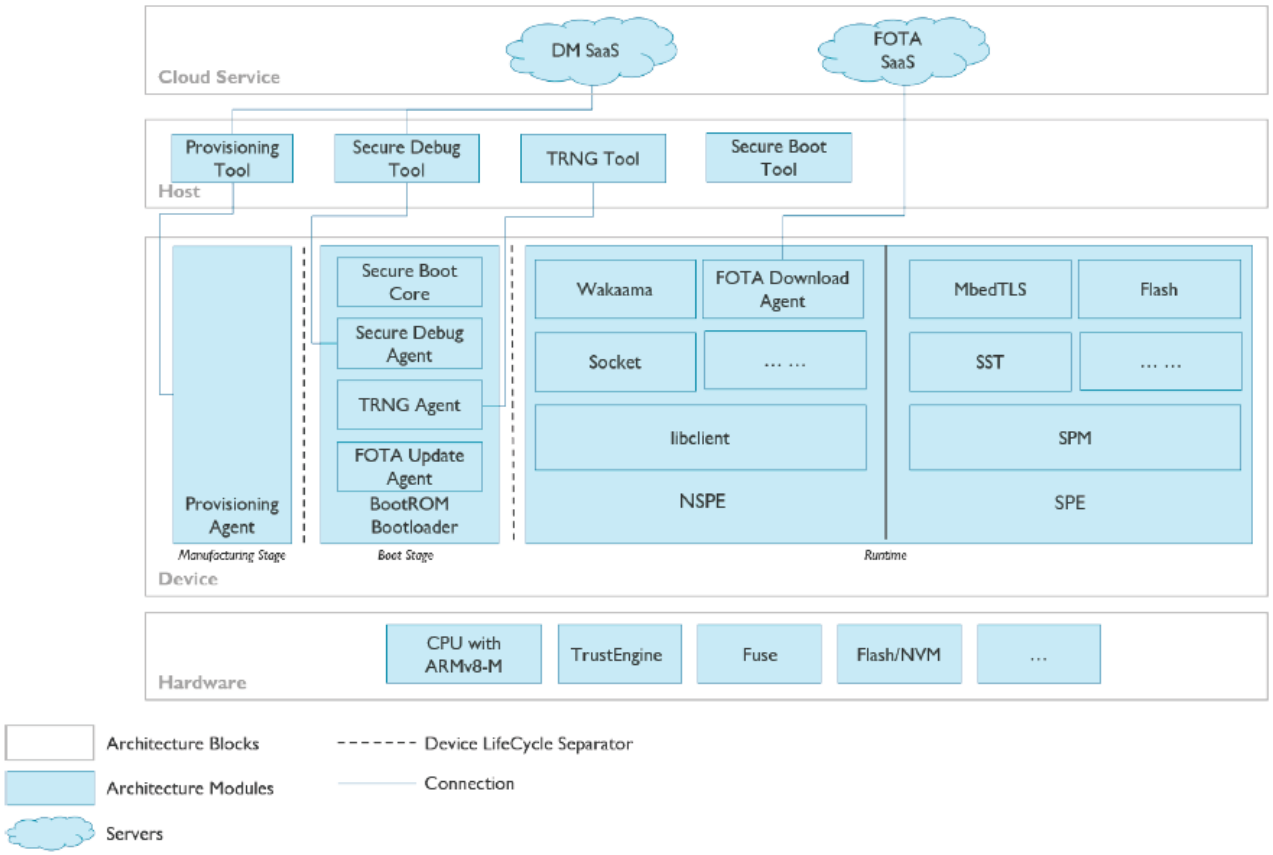
The IPSS software implements an all-round device-to-cloud security architecture, including:

- Provisioning mechanism in the manufacturing stage.
- Secure boot, secure debug, TRNG calibration, and FOTA update in the device boot stage.
- Secure connection and FOTA download in the device run-time stage.

IPSS also introduces a remote management solution to enable users to access, monitor and manage IoT devices in a secure manner. The remote management solution includes FOTA SaaS, Secure Debug SaaS, and Provisioning SaaS.

The following figure shows the architecture of the IPSS system.

Figure 4-4 Security Architecture of the IPSS System



4.24.1 Secure Boot

The secure boot solution provides the legitimacy and trustworthiness for images running on devices. It ensures that only official images which are published from OEMs are executable.

The secure boot functions include following aspects:

- Image verification
- Image encryption
- Extended program execution
- Image anti-rollback protection

4.24.2 Secure Debug

Secure debug provides a reliable mechanism for enabling the debug feature of a device after the device deployment.

Debug is one of the most commonly-used features in the device. With the debug feature, you can access all the device data, including the device firmware and the device root key.

4.24.3 FOTA

The FOTA solution implements a series of light-weight and trustworthy firmware upgrade interaction between IoT devices and servers, which includes downloading, verification, and installation.

4.24.4 Provisioning

Provisioning is the process to initialize secure credentials onto devices. It is required to happen in a secure environment such as the product line in the manufacturing stage.

The provisioning solution provides a full secure mechanism from the cloud server to devices. It keeps the security and integrity of provisioning materials, such as the device ID, model key, and the secure boot/secure debug public key hash, also keeps the device top secret such as the device root key that occurs only on the device side.

4.24.5 Secure Connection

The secure connection feature uses Mbed TLS to provide connection security in the transport layer over UDP. The key exchange method is Pre-Shared Key (PSK). The PSK's deployment happens in the manufacturing stage.

Mbed TLS provides cryptograph and SSL/TLS capabilities with TLS 1.1 and TLS 1.2.

4.24.6 BootROM

IPSS includes the BootROM reference code which is integrated with the secure boot solution.

There are primary boot and recovery boot paths in the BootROM.

- Primary boot is the main boot path. Normally devices should boot to the primary path.
- Recovery boot is the secondary boot path.

4.24.7 Bootloader

IPSS includes the Bootloader reference code which is integrated with the secure debug, provisioning, TRNG calibration, and FOTA solution.

In the primary bootloader, the secure debug agent, provisioning agent, and TRNG agent are integrated. The primary bootloader boots to the next image—TEE_M.

In the recovery bootloader, both the secure debug agent, TRNG agent, and the FOTA update agent are integrated. The recovery bootloader does not boot to any images.

4.24.8 TEE_M

IPSS introduces TEE_M. TEE_M provides an implementation of secure world software for Armv8-M, which follows Arm Platform Security Architecture (PSA) PSA_Firmware_Framework_1.0-bet0. IPSS TEE_M provides the following services by default:

- Secure Storage: The Secure Storage (Only supports Protected Storage) service supports PSA_Storage_API-1.0-bet2 without extended functions.
- Crypto: The Crypto service supports PSA_Cryptography_API_Reference_1.0_bet1.
- DTLS: DTLS (leverages Mbed TLS) is integrated in TEE_M.

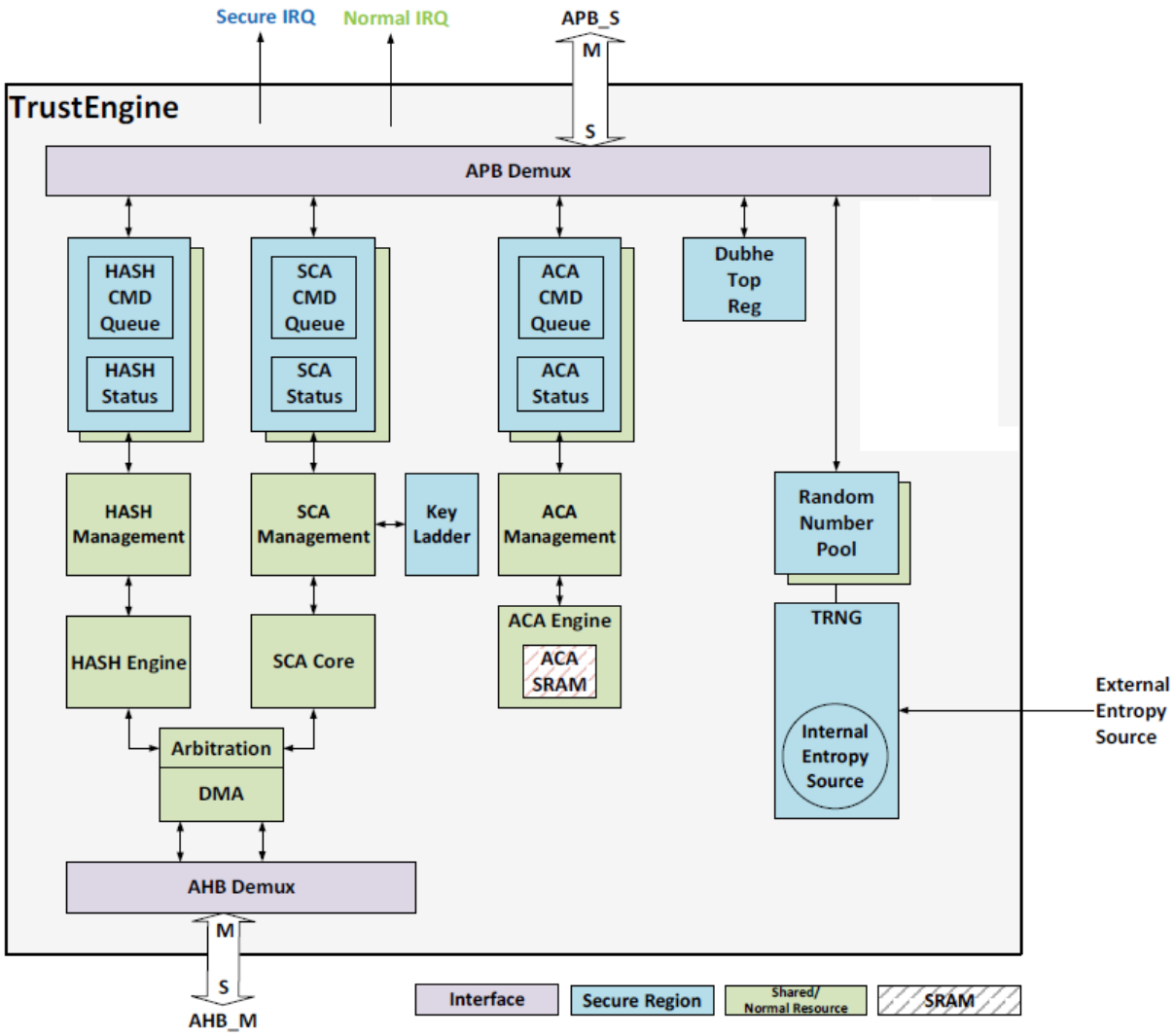
4.24.9 TrustEngine

IPSS introduces TrustEngine as a secure component in the system. It provides the following features:

- High security assurance. The crypto engine supports key ladders, lifecycle management and True Random Number Generator (TRNG) which enhance the system security.
- High performance and low power for encryption/decryption operation. This is achieved by TrustEngine internal cryptography engines.
- Reduction of software complicity in security. Some security functions are implemented in TrustEngine hardware, which can reduce the risk of sensitive information leakage to non-secure hosts.

The following figure shows the TrustEngine top-level architecture.

Figure 4-5 TrustEngine Top-Level Architecture



4.24.9.1 Features

TrustEngine includes the following features:

- Symmetric schemes, AES-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM (key size 128-bit, 192-bit and 256-bit)
- Symmetric schemes, SM4-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM
- Digest schemes, SHA1/224/256
- Digest scheme, SM3
- Asymmetric schemes, RSA 1024/2048/3072/4096 and ECCP 192/224/256/384/512/521
- Asymmetric scheme, SM2

- Key ladder for key management
- Lifecycle management
- True random number generator

4.24.9.2 Supported Standards and Specifications

TrustEngine is compliant with the following standards:

- FIPS PUB 180-4: Secure Hash Standard (SHS)
- FIPS PUB 197: Advanced Encryption Standard (AES)
- NIST SP 800-38A Recommendation for Block Cipher Modes of Operation-Methods and Techniques
- NIST SP 800-38B Recommendation for Block Cipher Modes of Operation: The CMAC Mode for Authentication
- NIST SP 800-38C Recommendation for Block Cipher Modes of Operation-the CCM Mode for Authentication and Confidentiality
- NIST SP 800-38D, Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC
- NIST SP 800-90B Recommendation for the Entropy Sources Used for Random Bit Generation
- SM2 Public Key Cryptographic Algorithm Based on Elliptic Curves (GB/T 32918-2016)
- SM3 Cryptographic Hash Algorithm (GB/T 32905-2016)
- SM4 Block Cipher Algorithm (GB/T 32907-2016)

4.24.9.3 Components

TrustEngine consists of five major function blocks.

- Symmetric Cryptography Accelerator (SCA)
- Asymmetric Cryptography Accelerator (ACA)
- HASH engine
- One-time programmable storage access controller
- True random number generator

Symmetric Cryptography Accelerator (SCA)

SCA in TrustEngine is responsible for data encryption/decryption using the symmetric cryptography algorithm. The data encryption/decryption operations are performed through the SCA engine by sending special commands to TrustEngine.

Asymmetric Cryptography Accelerator (ACA)

The ACA engine in TrustEngine is responsible for accelerating the asymmetric cryptography, such as:

- Asymmetric encryption and decryption: RSA and ECC
- Digital signature and verification: RSA signatures and ECDSA
- Key exchange: DH (Diffie-Hellman) and ECDH

HASH Accelerator

The HASH engine in TrustEngine is responsible for digest calculation. The digest of certain data can be calculated through the HASH engine by sending special commands to TrustEngine.

True Random Number Generator

The True Random Number Generator (TRNG) generates the random bits using the internal entropy source (ring oscillator inverter chain) or the external entropy source. The random bits are required by both secure and non-secure hosts.

5. Electrical Characteristics

Note: Values currently listed in this section are preliminary measurements and are subject to change.

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VBAT	Chip power supply voltage	-0.3	6.0	V
VIO	IO LDO output voltage	-0.3	4.0	V
VCCPA_2G	Supply voltage for 2.4 GHz RF PA	-0.3	4.0	V
VCCPAD_2G	Supply voltage for 2.4 GHz RF PA driver	-0.3	4.0	V
VCCPA_5G	Supply voltage for 5 GHz RF PA	-0.3	4.0	V
VCCPAD_5G	Supply voltage for 5 GHz RF PA driver	-0.3	4.0	V
VDD_FLASH	Supply voltage for external flash	-0.3	4.0	V
VDDA	Analog LDO output voltage	-0.3	1.8	V
	Analog buck output voltage	-0.3	1.8	V
VCCIF	Supply voltage for IF	-0.3	1.8	V
VCCRXFE	Supply voltage for RX	-0.3	1.8	V
VCCPLL_5G	Supply voltage for 5 GHz RF PLL	-0.3	1.8	V
VDDDIG	Digital core LDO output voltage	-0.3	1.1	V
VDDRAM	EXMEM LDO output voltage	-0.3	2.1	V
SWA	Analog buck switch output voltage	-0.3	4.0	V
P_{RX}	RX input power	-	10	dBm
T_{STR}	Storage temperature range	-55	150	°C

5.2 Recommended Operating Conditions

Parameter	Description	Min.(1)	Typ.	Max.	Unit
VBAT(2)	Chip power supply voltage	2.0	3.3	5.5	V
VBAT slew rate	-	300	-	-	mV/ms
VIO	IO LDO output voltage	2.0	3.0	3.6	V
VCCPA_2G(2)	Supply voltage for 2.4 GHz RF PA	2.0	3.0	3.6	V
VCCPAD_2G(2)	Supply voltage for 2.4 GHz RF PA driver	2.0	3.0	3.6	V
VCCPA_5G(2)	Supply voltage for 5 GHz RF PA	2.0	3.0	3.6	V
VCCPAD_5G(2)	Supply voltage for 5 GHz RF PA driver	2.0	3.0	3.6	V
VDD_FLASH	Supply voltage for external flash	2.0	3.0	3.6	V
VDDA	Analog LDO output voltage	-	1.5	-	V
	Analog buck output voltage	-	1.5	-	V
VCCIF	Supply voltage for IF	-	1.5	-	V
VCCRXFE	Supply voltage for RX	-	1.5	-	V
VCCPLL_5G	Supply voltage for 5 GHz RF PLL	-	1.5	-	V
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
VDDRAM	EXMEM LDO output voltage	1.8	-	1.95	V
T_{OPR}	Operating temperature range	-40	-	105	°C

(1) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. Care must be taken when operating at the minimum specified voltage.

(2) To ensure WLAN performance, the ripple on the supply must be less than Vpp = 100 mV.

5.3 Digital I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH	High-level input voltage	-	0.7 VIO	-	VIO + 0.3	V
VIL	Low-level input voltage	-	-0.3	-	0.3 VIO	V
VOH	High-level output voltage	-	0.8 VIO	-	-	V
VOL	Low-level output voltage	-	-	-	0.1 VIO	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	High-level source current	VOH = 0.8 VIO, GPIO_CAPACITY = 3	-	40	-	mA
		VOH = 0.8 VIO, GPIO_CAPACITY = 2	-	30	-	mA
		VOH = 0.8 VIO, GPIO_CAPACITY = 1	-	18	-	mA
		VOH = 0.8 VIO, GPIO_CAPACITY = 0	-	10	-	mA
I_{OL}	Low-level sink current	VOH = 0.15 VIO, GPIO_CAPACITY = 3	-	36	-	mA
		VOH = 0.15 VIO, GPIO_CAPACITY = 2	-	29	-	mA
		VOH = 0.15 VIO, GPIO_CAPACITY = 1	-	16	-	mA
		VOH = 0.15 VIO, GPIO_CAPACITY = 0	-	8	-	mA
R_{PU}	Weak pull-up resistor	-	-	40	-	kΩ
R_{PD}	Weak pull-down resistor	-	-	44	-	kΩ

5.4 IO LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VIO	IO LDO output voltage	2.0	3.0	3.6	V
Load current	-	-	-	300	mA

5.5 Analog LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog LDO output voltage	-	1.5	-	V
Load current	-	-	-	150	mA

5.6 Core LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
Load current	-	-	-	100	mA

5.7 EXMEM LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDRAM	EXMEM LDO output voltage	1.8	-	1.95	V
Load current	-	-	-	50	mA

5.8 Analog Buck

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog buck output voltage	-	1.5	-	V
Load current	-	-	-	150	mA
Switching frequency	Buck modulation frequency	0.5	1	2	MHz
Output filter capacitor capacitance	-	-	4.7	-	μF
Inductor inductance	-	-	4.7	-	μH
Inductor DC resistance	-	-	-	500	mΩ
Inductor saturation current	-	200	-	-	mA

5.9 40 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal frequency	-	-	40	-	MHz
ΔF/F0	Frequency tolerance	25 °C	-10	-	+10	ppm
TC		-40 to 105 °C crystal	-20	-	+20	ppm

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Frequency stability over operating temperature	-30 to 85 °C crystal	-10	-	+10	ppm
CL	Load capacitance	-	7	8	9	pF
TS	Trim sensitivity	-40 to 105 °C crystal	-	26	-	ppm/pF
		-30 to 85 °C crystal	-	26	-	ppm/pF

5.10 32.768 kHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal frequency	-	-	32.768	-	kHz
ΔF/F0	Frequency tolerance	25 °C	-20	-	+20	ppm
T_{OPR}	Operating temperature range	-	-40	-	85	°C
CL	Load capacitance	-	-	12.5	-	pF
ESR	Equivalent series resistance	25 °C	-	-	70	kΩ

5.11 Current Consumption

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Band	Condition	Min.	Typ.	Max.	Unit
Active Mode						
RX current	2.4 GHz	-	-	9	-	mA
	5 GHz	-	-	16	-	mA
TX current	WLAN 2.4 GHz	11b: 11 Mbps DSSS @ 19 dBm	-	265	-	mA
		11g: 54 Mbps OFDM @ 17 dBm	-	230	-	mA
		11n: MCS7, HT20 @ 16 dBm	-	215	-	mA
		11n: MCS7, HT40 @ 15 dBm	-	210	-	mA
		11ax: MCS7, HE20 @ 16 dBm	-	220	-	mA
		11a: 54 Mbps OFDM @ 17 dBm	-	320	-	mA

Parameter	Band	Condition	Min.	Typ.	Max.	Unit
	WLAN 5 GHz	11n: MCS7, HT20 @ 16 dBm	-	310	-	mA
		11ax: MCS7, HE20 @ 16 dBm	-	305	-	mA
	Bluetooth LE	15 dBm	-	180	-	mA
		6 dBm	-	110	-	mA
		0 dBm	-	100	-	mA
		-15 dBm	-	95	-	mA
Sleep Mode						
Sleep	-	-	-	19	-	μA
Deep sleep	-	-	-	0.7	-	μA
Shutdown Mode						
Shutdown	-	-	-	0.2	-	μA

5.12 RF Characteristics

Unless otherwise noted, the RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The front-end circuit is a matching network designed to ensure that the product complies with wireless regulations in various countries.

5.12.1 WLAN RF Characteristics

5.12.1.1 WLAN 2.4 GHz Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b (8% PER)	1 Mbps DSSS	-	-100	-	dBm
	2 Mbps DSSS	-	-96	-	dBm
	5.5 Mbps DSSS	-	-93	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
	11 Mbps DSSS	-	-91	-	dBm
Sensitivity - IEEE 802.11g (10% PER)	6 Mbps OFDM	-	-93	-	dBm
	9 Mbps OFDM	-	-92	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-89	-	dBm
	24 Mbps OFDM	-	-86	-	dBm
	36 Mbps OFDM	-	-83	-	dBm
	48 Mbps OFDM	-	-79	-	dBm
	54 Mbps OFDM	-	-78	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz (10% PER)	HT20, MCS0	-	-92	-	dBm
	HT20, MCS1	-	-92	-	dBm
	HT20, MCS2	-	-89	-	dBm
	HT20, MCS3	-	-87	-	dBm
	HT20, MCS4	-	-83	-	dBm
	HT20, MCS5	-	-79	-	dBm
	HT20, MCS6	-	-77	-	dBm
	HT20, MCS7	-	-76	-	dBm
Sensitivity - IEEE 802.11n, 40 MHz (10% PER)	HT40, MCS0	-	-89	-	dBm
	HT40, MCS1	-	-87	-	dBm
	HT40, MCS2	-	-86	-	dBm
	HT40, MCS3	-	-83	-	dBm
	HT40, MCS4	-	-80	-	dBm
	HT40, MCS5	-	-76	-	dBm
	HT40, MCS6	-	-75	-	dBm
	HT40, MCS7	-	-72	-	dBm
Sensitivity - IEEE 802.11ax, 20 MHz (10% PER)	HE20, MCS0	-	-92	-	dBm
	HE20, MCS1	-	-90	-	dBm
	HE20, MCS2	-	-88	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
	HE20, MCS3		-	-86	-	dBm
	HE20, MCS4		-	-82	-	dBm
	HE20, MCS5		-	-78	-	dBm
	HE20, MCS6		-	-76	-	dBm
	HE20, MCS7		-	-75	-	dBm
	HE20, MCS8		-	-71	-	dBm
	HE20, MCS9		-	-69	-	dBm
Maximum Receive Level						
Maximum receive level @ 2.4 GHz	11b: 1 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11b: 11 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11g: 6 Mbps (10% PER, 1000 octets)		-	10	-	dBm
	11g: 54 Mbps (10% PER, 1000 octets)		-	5	-	dBm
	11n: HT20 MCS0 (10% PER, 4096 octets)		-	10	-	dBm
	11n: HT20 MCS7 (10% PER, 4096 octets)		-	5	-	dBm
	11n: HT40 MCS0 (10% PER, 4096 octets)		-	5	-	dBm
	11n: HT40 MCS7 (10% PER, 4096 octets)		-	0	-	dBm
	11ax: HE20 MCS0 (10% PER, 4096 octets)		-	0	-	dBm
	11ax: HE20 MCS9 (10% PER, 4096 octets)		-	-5	-	dBm
Adjacent Channel Rejection						
Adjacent channel (±30 MHz) rejection - IEEE 802.11b (8% PER with desired signal level as specified in Condition)	1 Mbps DSSS	-74 dBm	-	46	-	dB
	2 Mbps DSSS	-74 dBm	-	44	-	dB

Parameter	Condition		Min.	Typ.	Max.	Unit
Adjacent channel (±25 MHz) rejection - IEEE 802.11b	5.5 Mbps DSSS	-70 dBm	-	40	-	dB
(8% PER with desired signal level as specified in Condition)	11 Mbps DSSS	-70 dBm	-	40	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11g	6 Mbps OFDM	-79 dBm	-	41	-	dB
(10% PER with desired signal level as specified in Condition)	54 Mbps OFDM	-62 dBm	-	29	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11n	HT20, MCS0	-79 dBm	-	40	-	dB
(10% PER with desired signal level as specified in Condition)	HT20, MCS7	-61 dBm	-	26	-	dB
Adjacent channel (±40 MHz) rejection - IEEE 802.11n	HT40, MCS0	-76 dBm	-	37	-	dB
(10% PER with desired signal level as specified in Condition)	HT40, MCS7	-58 dBm	-	20	-	dB
Adjacent channel (±20 MHz) rejection - IEEE 802.11ax	HE20, MCS0	-79 dBm	-	40	-	dB
(10% PER with desired signal level as specified in Condition)	HE20, MCS9	-54 dBm	-	23	-	dB
Spurious Emissions						
Spurious emissions	< 1 GHz		-	-	-60	dBm
	> 1 GHz		-	-	-55	dBm

5.12.1.2 WLAN 2.4 GHz Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
TX Power					
TX power - IEEE 802.11b	1 Mbps DSSS	-	21	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
(SEM compliant)	11 Mbps DSSS	-	21	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM	-	19	-	dBm
	54 Mbps OFDM	-	18	-	dBm
TX power - IEEE 802.11n (EVM compliant)	HT20, MCS0	-	18	-	dBm
	HT20, MCS7	-	17	-	dBm
	HT40, MCS0	-	16	-	dBm
	HT40, MCS7	-	15	-	dBm
TX power - IEEE 802.11ax (EVM compliant)	HE20, MCS0	-	18	-	dBm
	HE20, MCS9	-	14	-	dBm
Spurious Emissions					
Spurious emissions (at maximum output power)	< 1 GHz	-	-55	-	dBm
	> 1 GHz	-	-45	-	dBm

5.12.1.3 WLAN 5 GHz Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	4900	-	5925	MHz
Sensitivity					
Sensitivity - IEEE 802.11a (10% PER)	6 Mbps OFDM	-	-92	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-90	-	dBm
	18 Mbps OFDM	-	-89	-	dBm
	24 Mbps OFDM	-	-86	-	dBm
	36 Mbps OFDM	-	-83	-	dBm
	48 Mbps OFDM	-	-79	-	dBm
	54 Mbps OFDM	-	-77	-	dBm
	HT20, MCS0	-	-92	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity - IEEE 802.11n, 20 MHz (10% PER)	HT20, MCS1	-	-90	-	dBm
	HT20, MCS2	-	-88	-	dBm
	HT20, MCS3	-	-85	-	dBm
	HT20, MCS4	-	-81	-	dBm
	HT20, MCS5	-	-77	-	dBm
	HT20, MCS6	-	-75	-	dBm
	HT20, MCS7	-	-74	-	dBm
Sensitivity - IEEE 802.11n, 40 MHz (10% PER)	HT40, MCS0	-	-88	-	dBm
	HT40, MCS1	-	-87	-	dBm
	HT40, MCS2	-	-85	-	dBm
	HT40, MCS3	-	-82	-	dBm
	HT40, MCS4	-	-79	-	dBm
	HT40, MCS5	-	-74	-	dBm
	HT40, MCS6	-	-73	-	dBm
	HT40, MCS7	-	-72	-	dBm
Sensitivity - IEEE 802.11ac, 20 MHz (10% PER)	VHT20, MCS0	-	-92	-	dBm
	VHT20, MCS1	-	-90	-	dBm
	VHT20, MCS2	-	-88	-	dBm
	VHT20, MCS3	-	-85	-	dBm
	VHT20, MCS4	-	-82	-	dBm
	VHT20, MCS5	-	-78	-	dBm
	VHT20, MCS6	-	-76	-	dBm
	VHT20, MCS7	-	-74	-	dBm
Sensitivity - IEEE 802.11ax, 20 MHz (10% PER)	HE20, MCS0	-	-92	-	dBm
	HE20, MCS1	-	-90	-	dBm
	HE20, MCS2	-	-88	-	dBm
	HE20, MCS3	-	-85	-	dBm
	HE20, MCS4	-	-81	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
	HE20, MCS5		-	-77	-	dBm
	HE20, MCS6		-	-75	-	dBm
	HE20, MCS7		-	-73	-	dBm
	HE20, MCS8		-	-69	-	dBm
	HE20, MCS9		-	-67	-	dBm
Maximum Receive Level						
Maximum receive level @ 5 GHz	11a: 6 Mbps (10% PER, 1000 octets)		-	10	-	dBm
	11a: 54 Mbps (10% PER, 1000 octets)		-	TBD	-	dBm
	11n: HT20 MCS0 (10% PER, 4096 octets)		-	10	-	dBm
	11n: HT20 MCS7 (10% PER, 4096 octets)		-	TBD	-	dBm
	11n: HT40 MCS0 (10% PER, 4096 octets)		-	TBD	-	dBm
	11n: HT40 MCS7 (10% PER, 4096 octets)		-	TBD	-	dBm
	11ac: VHT20 MCS0 (10% PER, 4096 octets)		-	TBD	-	dBm
	11ac: VHT20 MCS7 (10% PER, 4096 octets)		-	TBD	-	dBm
	11ax: HE20 MCS0 (10% PER, 4096 octets)		-	10	-	dBm
	11ax: HE20 MCS9 (10% PER, 4096 octets)		-	TBD	-	dBm
Adjacent Channel Rejection						
Adjacent channel (±20 MHz) rejection - IEEE 802.11a (10% PER with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	-	TBD	-	dB
	54 Mbps OFDM	-62 dBm	-	TBD	-	dB
Adjacent channel (±20 MHz) rejection - IEEE 802.11n	HT20, MCS0	-79 dBm	-	TBD	-	dB

Parameter	Condition		Min.	Typ.	Max.	Unit
(10% PER with desired signal level as specified in Condition)	HT20, MCS7	-61 dBm	-	TBD	-	dB
Adjacent channel (±40 MHz) rejection - IEEE 802.11n	HT40, MCS0	-76 dBm	-	TBD	-	dB
(10% PER with desired signal level as specified in Condition)	HT40, MCS7	-58 dBm	-	TBD	-	dB
Adjacent channel (±20 MHz) rejection - IEEE 802.11ac	VHT20, MCS0	-79 dBm	-	TBD	-	dB
(10% PER with desired signal level as specified in Condition)	VHT20, MCS7	-61 dBm	-	TBD	-	dB
Adjacent channel (±20 MHz) rejection - IEEE 802.11ax	HE20, MCS0	-79 dBm	-	TBD	-	dB
(10% PER with desired signal level as specified in Condition)	HE20, MCS9	-54 dBm	-	TBD	-	dB
Nonadjacent Channel Rejection						
Nonadjacent channel (±40 MHz) rejection - IEEE 802.11a	6 Mbps OFDM	-79 dBm	-	TBD	-	dB
(10% PER with desired signal level as specified in Condition)	54 Mbps OFDM	-62 dBm	-	TBD	-	dB
Nonadjacent channel (±40 MHz) rejection - IEEE 802.11n	HT20, MCS0	-79 dBm	-	TBD	-	dB
(10% PER with desired signal level as specified in Condition)	HT20, MCS7	-61 dBm	-	TBD	-	dB
Nonadjacent channel (±80 MHz) rejection - IEEE 802.11n	HT40, MCS0	-76 dBm	-	TBD	-	dB
(10% PER with desired signal level as specified in Condition)	HT40, MCS7	-58 dBm	-	TBD	-	dB
Nonadjacent channel (±40 MHz) rejection - IEEE 802.11ac	VHT20, MCS0	-79 dBm	-	TBD	-	dB
(10% PER with desired signal level as specified in Condition)	VHT20, MCS7	-61 dBm	-	TBD	-	dB
Nonadjacent channel (±40 MHz) rejection - IEEE 802.11ax	HE20, MCS0	-79 dBm	-	TBD	-	dB

Parameter	Condition		Min.	Typ.	Max.	Unit
(10% PER with desired signal level as specified in Condition)	HE20, MCS9	-54 dBm	-	TBD	-	dB
Spurious Emissions						
Spurious emissions	< 1 GHz		-	-	-60	dBm
	> 1 GHz		-	-	-55	dBm

5.12.1.4 WLAN 5 GHz Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	4900	-	5925	MHz
TX Power					
TX power - IEEE 802.11a (EVM compliant)	6 Mbps OFDM	-	18	-	dBm
	54 Mbps OFDM	-	16	-	dBm
TX power - IEEE 802.11n (EVM compliant)	HT20, MCS0	-	17	-	dBm
	HT20, MCS7	-	15	-	dBm
	HT40, MCS0	-	15	-	dBm
	HT40, MCS7	-	14	-	dBm
TX power - IEEE 802.11ac (EVM compliant)	VHT20, MCS0	-	17	-	dBm
	VHT20, MCS7	-	15	-	dBm
TX power - IEEE 802.11ax (EVM compliant)	HE20, MCS0	-	17	-	dBm
	HE20, MCS9	-	13	-	dBm
Spurious Emissions					
Spurious emissions (at maximum output power)	< 1 GHz	-	-55	-	dBm
	> 1 GHz	-	-45	-	dBm

5.12.2 Bluetooth LE RF Characteristics

5.12.2.1 Bluetooth LE Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-98	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	7	-	dB
C/I 1 MHz adjacent channel	-	-	0	-	dB
C/I -1 MHz adjacent channel	-	-	0	-	dB
C/I 2 MHz adjacent channel	-	-	-25	-	dB
C/I -2 MHz adjacent channel	-	-	-33	-	dB
C/I 3 MHz adjacent channel	-	-	-30	-	dB
C/I -3 MHz adjacent channel	-	-	-40	-	dB
C/I > 3 MHz adjacent channel	-	-	-48	-	dB
C/I < -3 MHz adjacent channel	-	-	-48	-	dB
Out-of-band blocking	30–2000 MHz	-	TBD	-	dBm
	2003–2399 MHz	-	TBD	-	dBm
	2484–2997 MHz	-	TBD	-	dBm
	3000 MHz–12.75 GHz	-	TBD	-	dBm
Intermodulation	-	-	TBD	-	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	-95	-	dBm
Maximum input level	30.8% PER	-	TBD	-	dBm
C/I co-channel	-	-	TBD	-	dB
C/I 2 MHz adjacent channel	-	-	TBD	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I -2 MHz adjacent channel	-	-	TBD	-	dB
C/I 4 MHz adjacent channel	-	-	TBD	-	dB
C/I -4 MHz adjacent channel	-	-	TBD	-	dB
C/I 6 MHz adjacent channel	-	-	TBD	-	dB
C/I -6 MHz adjacent channel	-	-	TBD	-	dB
C/I > 6 MHz adjacent channel	-	-	TBD	-	dB
C/I < -6 MHz adjacent channel	-	-	TBD	-	dB
Out-of-band blocking	30–2000 MHz	-	TBD	-	dBm
	2003–2399 MHz	-	TBD	-	dBm
	2484–2997 MHz	-	TBD	-	dBm
	3000 MHz–12.75 GHz	-	TBD	-	dBm
Intermodulation	-	-	TBD	-	dBm
Bluetooth LE 125 kbps					
Sensitivity	30.8% PER	-	TBD	-	dBm
Maximum input level	30.8% PER	-	TBD	-	dBm
C/I co-channel	-	-	TBD	-	dB
C/I 1 MHz adjacent channel	-	-	TBD	-	dB
C/I -1 MHz adjacent channel	-	-	TBD	-	dB
C/I 2 MHz adjacent channel	-	-	TBD	-	dB
C/I -2 MHz adjacent channel	-	-	TBD	-	dB
C/I 3 MHz adjacent channel	-	-	TBD	-	dB
C/I -3 MHz adjacent channel	-	-	TBD	-	dB
C/I > 3 MHz adjacent channel	-	-	TBD	-	dB
C/I < -3 MHz adjacent channel	-	-	TBD	-	dB
Bluetooth LE 500 kbps					
Sensitivity	30.8% PER	-	TBD	-	dBm
Maximum input level	30.8% PER	-	TBD	-	dBm
C/I co-channel	-	-	TBD	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I 1 MHz adjacent channel	-	-	TBD	-	dB
C/I -1 MHz adjacent channel	-	-	TBD	-	dB
C/I 2 MHz adjacent channel	-	-	TBD	-	dB
C/I -2 MHz adjacent channel	-	-	TBD	-	dB
C/I 3 MHz adjacent channel	-	-	TBD	-	dB
C/I -3 MHz adjacent channel	-	-	TBD	-	dB
C/I > 3 MHz adjacent channel	-	-	TBD	-	dB
C/I < -3 MHz adjacent channel	-	-	TBD	-	dB

5.12.2.2 Bluetooth LE Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter		Condition	Min.	Typ.	Max.	Unit
General						
Frequency range		-	2402	-	2480	MHz
TX power		-	-20	6	25	dBm
Bluetooth LE 1 Mbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-50	-	dBm
	>±3 MHz offset	-	-	-52	-	dBm
Modulation characteristics	Δf1avg	-	225	250	275	kHz
	Δf2max	-	185	235	-	kHz
	Δf2avg/Δf1avg	-	0.8	1	-	-
Carrier frequency offset and drift	Max $\lvert f_n \rvert$ $n = 0, 1, 2, 3 \ldots k$	-	-	3	150	kHz
	Max $\lvert f_0 - f_n \rvert$ $n = 2, 3, 4 \ldots k$	-	-	2.5	50	kHz
	$\lvert f_1 - f_0 \rvert$	-	-	2	23	kHz
	Max $\lvert f_n - f_{n-5} \rvert$ $n = 6, 7, 8 \ldots k$	-	-	2.5	20	kHz/50 μs
Bluetooth LE 2 Mbps						
	±4 MHz offset	-	-	-50	-	dBm

Parameter		Condition	Min.	Typ.	Max.	Unit
In-band emissions	±5 MHz offset	-	-	-51	-	dBm
	>±5 MHz offset	-	-	-52	-	dBm
Modulation characteristics	Δf1avg	-	-	478	-	kHz
	Δf2max	-	-	495	-	kHz
	Δf2avg/Δf1avg	-	-	1	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	3	150	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	2.5	50	kHz
	$\|f_1 - f_0\|$	-	-	1.5	23	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	2.5	20	kHz/50 μs
Bluetooth LE 125 kbps						
In-band emissions	±2 MHz offset	-	-	TBD	-	dBm
	±3 MHz offset	-	-	TBD	-	dBm
	>±3 MHz offset	-	-	TBD	-	dBm
Modulation characteristics	Δf1avg	-	225	TBD	275	kHz
	Δf1max	-	185	TBD	-	kHz
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	TBD	150	kHz
	Max $\|f_0 - f_n\|$ n = 1, 2, 3…k	-	-	TBD	50	kHz
	$\|f_0 - f_3\|$	-	-	TBD	19.2	kHz
	$\|f_n - f_{n-3}\|$ n = 7, 8, 9…k	-	-	TBD	19.2	kHz/48 μs
Bluetooth LE 500 kbps						
In-band emissions	±2 MHz offset	-	-	TBD	-	dBm
	±3 MHz offset	-	-	TBD	-	dBm
	>±3 MHz offset	-	-	TBD	-	dBm

5.12.3 IEEE 802.15.4 RF Characteristics

5.12.3.1 IEEE 802.15.4 Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2400	-	2483.5	MHz
O-QPSK 250 kbps					
Sensitivity	1 % PER	-	-104	-	dBm
Maximum input level	1 % PER	-	TBD	-	dBm
Co-channel rejection	1 % PER, desired signal @ -82 dBm	-	TBD	-	dB
Adjacent channel (+5 MHz) rejection	1 % PER, desired signal @ -82 dBm	-	TBD	-	dB
Adjacent channel (-5 MHz) rejection	1 % PER, desired signal @ -82 dBm	-	TBD	-	dB
Alternate channel (+10 MHz) rejection	1 % PER, desired signal @ -82 dBm	-	TBD	-	dB
Alternate channel (-10 MHz) rejection	1 % PER, desired signal @ -82 dBm	-	TBD	-	dB
Channel (+15 MHz) rejection	1 % PER, desired signal @ -82 dBm	-	TBD	-	dB
Channel (-15 MHz) rejection	1 % PER, desired signal @ -82 dBm	-	TBD	-	dB
Spurious emissions	< 1 GHz	-	-	-60	dBm
	> 1 GHz	-	-	-55	dBm

5.12.3.2 IEEE 802.15.4 Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2400	-	2483.5	MHz

Parameter	Condition	Min.	Typ.	Max.	Unit
O-QPSK 250 kbps					
Maximum output power	-	-	15	-	dBm
Error-vector magnitude (EVM)	-	-	TBD	-	%
Center frequency tolerance	-	-	TBD	-	ppm
Power spectral density (PSD)	Relative, at greater than 3.5 MHz offset	-	TBD	-	dB
	Absolute, at greater than 3.5 MHz offset	-	TBD	-	dBm
Spurious emissions	30–1000 MHz	-	-55	-	dBm
	1–12.75 GHz	-	-45	-	dBm

5.13 AUX ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Conversion clock	-	1.33	-	40	MHz
Conversion time	-	-	26	-	Cycle
V_{REF}	Internal	-	1.5 or 1.8	-	V
	External	-	VIO/2	-	V
Input voltage range	-	0	-	V_{REF}*2	V
Input impedance	-	10	-	-	MΩ
Input capacitance (Cs)	-	-	4	-	pF
DNL	-	-	±0.5	-	LSB
INL	-	-	±1	-	LSB
ENOB	-	-	12	-	Bit
SNDR	-	-	74	-	dB
SFDR	-	-	84	-	dB
$T_{STARTUP}$	-	-	5	-	μs
Current consumption	-	-	1	-	mA

6. Package Information

6.1 QFN48 6 x 6 x 0.75 mm Package

Figure 6-1 QFN48 6 x 6 x 0.75 mm Package Outline

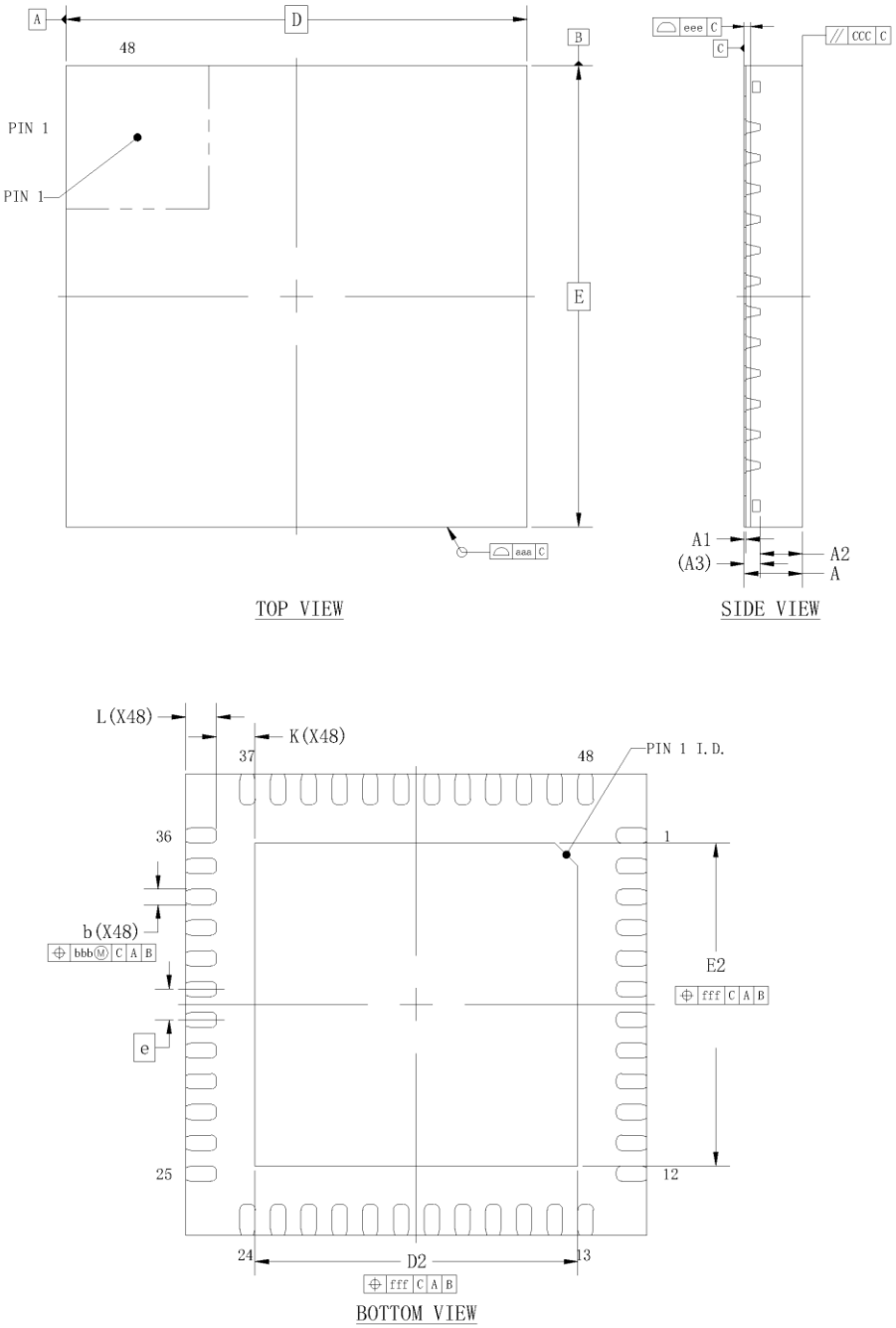


Table 6-1 QFN48 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
D2	4.10	4.20	4.30
E2	4.10	4.20	4.30
L	0.30	0.40	0.50
K	0.50 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
eee	0.08		
fff	0.10		

6.2 QFN40 5 x 5 x 0.75 mm Package

Figure 6-2 QFN40 5 x 5 x 0.75 mm Package Outline

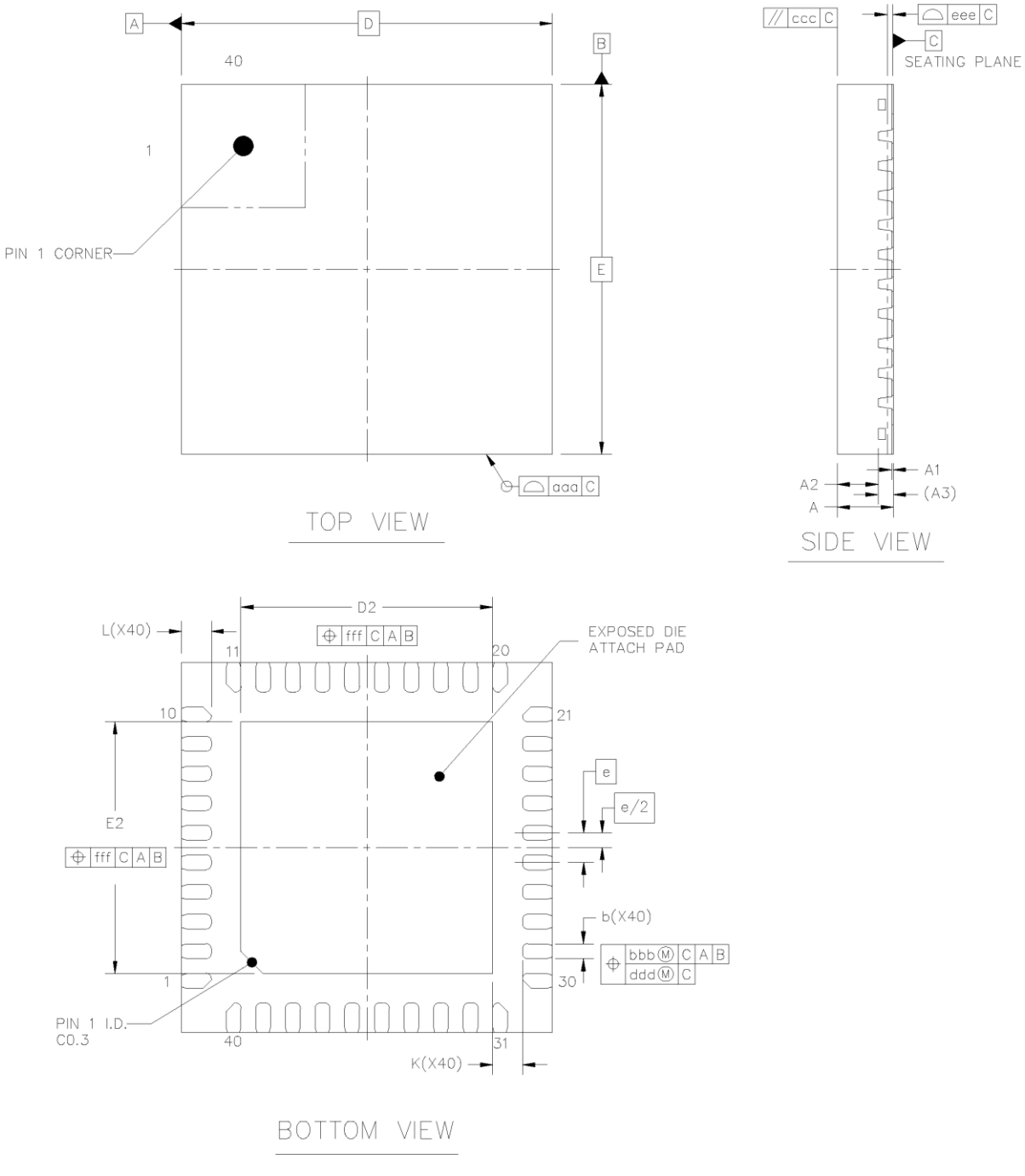
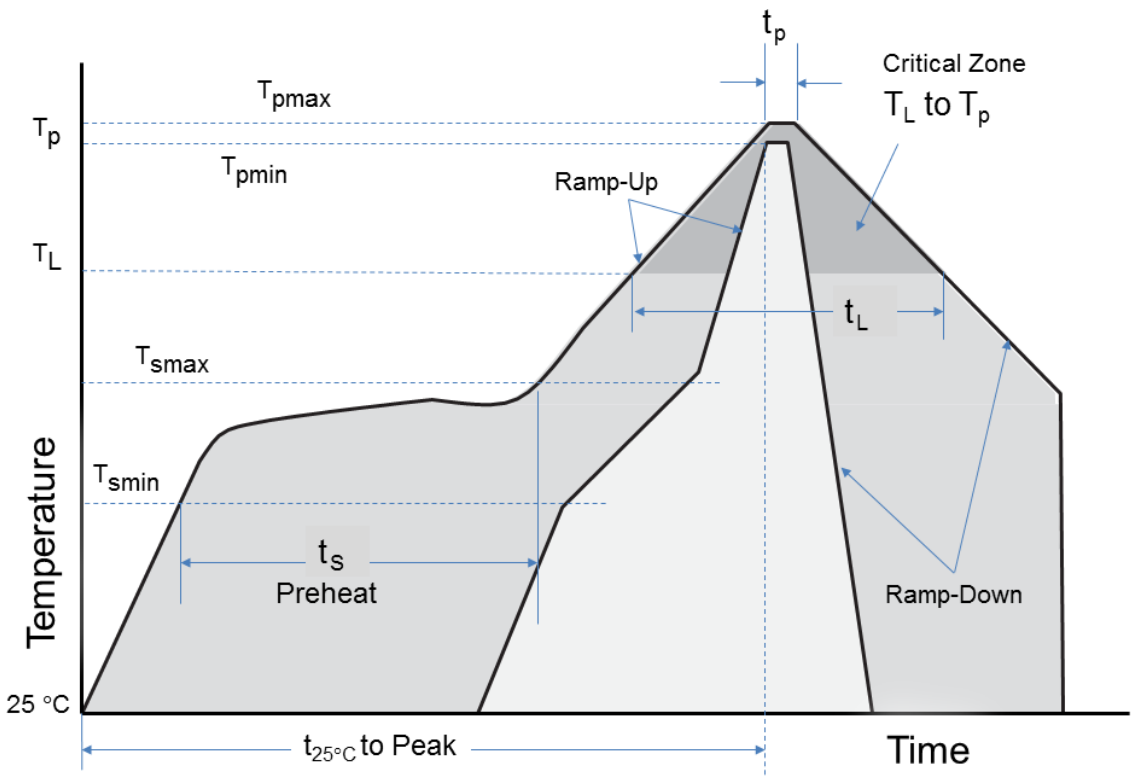


Table 6-2 QFN40 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
D2	3.30	3.40	3.50
E2	3.30	3.40	3.50
L	0.30	0.40	0.50
K	0.40 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
ddd	0.05		
fff	0.10		

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 °C/s max.
Preheat	Temperature min. (T_{smin})	150 °C
	Temperature max. (T_{smax})	200 °C
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 °C
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 °C
Time within 5 °C of actual peak temperature (t_p)		20 s to 40 s
Ramp-down rate		6 °C/s max.

Profile Feature	Specification
Time 25 °C to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, or DIBP content in accordance with EU RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Figure 8-1 Ordering Code Scheme

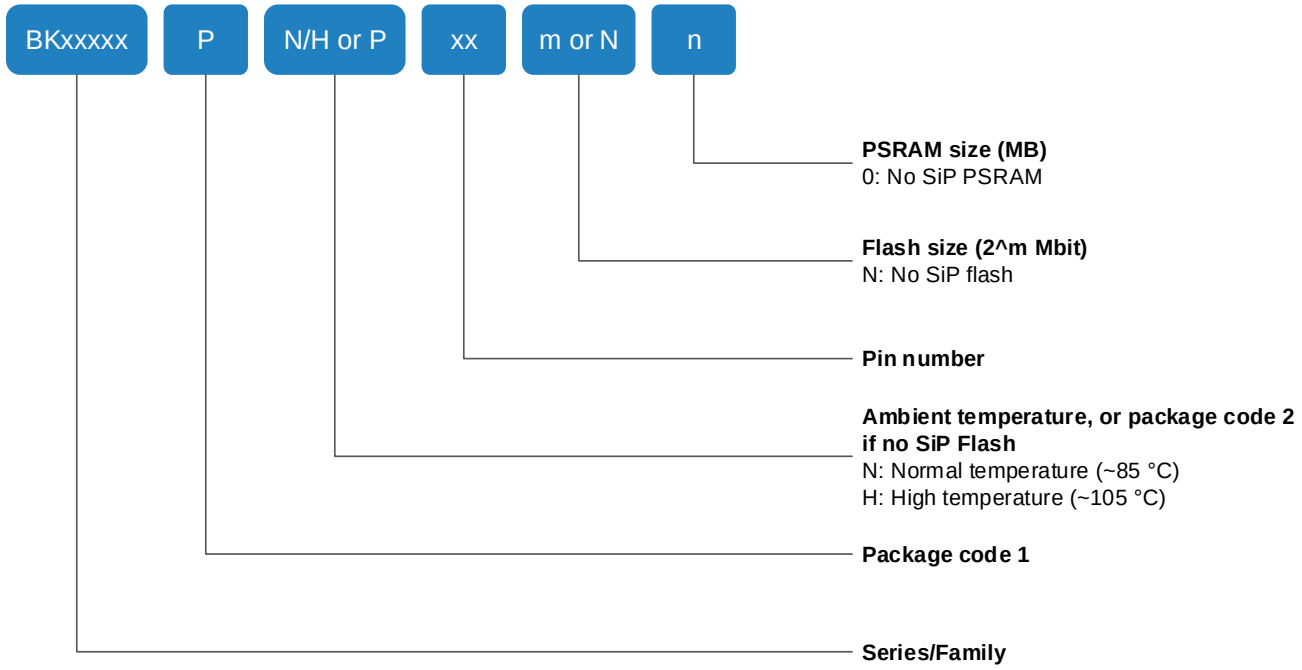


Table 8-1 Ordering Information

Ordering Code	Package	SiP(1) Flash	SiP PSRAM	Packing	Minimum Ordering Qty (MOQ)(2)
BK7239NQN48N8	6 mm x 6 mm x 0.75 mm QFN48	-	8 MB	Tape and Reel	3000
BK7239NQH4050	5 mm x 5 mm x 0.75 mm QFN40	4 MB	-	Tape and Reel	3000

(1) A system in a package (SiP) refers to flash/PSRAM enclosed in the package.

(2) The MOQ for customized or exclusive ordering codes is one wafer lot. Please consult your sales representative for the exact quantity.

Revision History

Version	Date	Description
1.0	2024/6/27	Initial release
1.1	2024/8/19	• Added Wi-Fi 6E support • Added IEEE 802.15.4 features and updated current values in Section 1 Features • Added QFN48 package • Updated the name of pin 5 for the QFN56 package in Section 3 Pin Descriptions • Updated the description of Section 4.2 RF Transceivers • Updated the description of Section 4.5 Reset • Updated VDDA voltage and VDDDIG voltage in Figure 4-1 in Section 4.6.1 Power Scheme • Update the description of sleep mode in Section 4.6.2 Power Modes • Updated UART baud rate in Section 4.11 UART Interfaces (UART) • Updated the maximum voltage of VCCIF, VCCRXFE, VCCPLL_2G, VCCPLL_5G, VCCA, VDDA, and VDDDIG in Section 5.1 Absolute Maximum Ratings • Added the typical voltage of VCCIF, VCCRXFE, VCCPLL_2G, VCCPLL_5G, VCCA, VDDA, and VDDDIG in Section 5.2 Recommended Operating Conditions • Updated VDDA (LDO output) typical voltage in Section 5.5 Analog LDO • Updated VDDDIG typical voltage in Section 5.6 Core LDO • Updated VDDA (buck output) typical voltage in Section 5.8 Analog Buck • Updated the load capacitance and trim sensitivity of the 40 MHz crystal in Section 5.9 40 MHz Crystal Characteristics • Updated and added current values in Section 5.11 Current Consumption • Updated and added RF characteristics values in Section 5.12.1 WLAN RF Characteristics
1.2	2025/4/29	• Removed Wi-Fi 6 GHz band support and Wi-Fi 6E support • Added support of 40 MHz channel bandwidth for 2.4 GHz and 5 GHz • Updated SRAM size • Updated maximum VBAT voltage

Version	Date	Description
		• Removed QFN56 package and updated QFN48 package pin assignments • Updated maximum operating temperature • Updated I/O pin multiplexing in Section 3.3 Pin Multiplexing • Changed the heading of Section 4.1 to IEEE 802.15.4 Overview • Updated the description of watchdog reset in Section 4.5 Reset • Updated Section 4.6.1 Power Scheme • Modified the description of wake-up sources for deep sleep and sleep modes in Section 4.6.2 Power Modes • Added Section 4.7 I/O Multiplexer (IOMUX) • Updated the description of Section 4.8 General-purpose I/Os (GPIO) • Added the description of UART0 flash download in Section 4.11 UART Interfaces (UART) • Updated the introduction to PWM module in Section 4.16 PWM Module (PWM) • Section 4.18 Auxiliary ADC (AUX ADC): – Updated conversion modes – Updated sampling rate range – Updated external analog input channels and internal channels • Updated Section 5.1 Absolute Maximum Ratings • Updated Section 5.2 Recommended Operating Conditions • Updated the minimum value of VOH in Section 5.3 Digital I/O Characteristics • Added Section 5.4 IO LDO • Updated VDDA (LDO output) typical voltage in Section 5.5 Analog LDO • Updated VDDA (buck output) typical voltage in Section 5.8 Analog Buck • Updated Section 5.11 Current Consumption • Updated Section 5.12.1 WLAN RF Characteristics • Updated conversion clock and external V_{REF} voltage for AUX ADC in Section 5.13 AUX ADC Characteristics • Section 8 Ordering Information: – Updated the title of Figure 8-1 – Updated ordering code – Added a note about MOQ in Table 8-1
1.3	2025/6/17	• Updated Section 5.11 Current Consumption • Updated Section 5.12.1 WLAN RF Characteristics

Version	Date	Description

1.4	2025/6/27	• Section 1 Features:
		  – Added description for 802.11ax MCS support
		  – Added description for flash XIP support
		  – Updated current values
		• Added QFN40 package
		• Updated maximum operating temperature
		• Corrected WDT clock source in Section 4.20 Watchdog Timer (WDT)
		• Corrected RTC clock sources in Section 4.21 Real-time Counter (RTC)
		• Corrected VDDDIG maximum voltage rating to 1.1 V in Section 5.1 Absolute Maximum Ratings
		• Updated I/O output current values in Section 5.3 Digital I/O Characteristics
		• Added Section 5.7 EXMEM LDO
		• Updated Section 5.11 Current Consumption
		• Added sensitivity values for 802.11ax HE20 MCS8 and MCS9 in Section 5.12.1.1 WLAN 2.4 GHz Receiver Characteristics and Section 5.12.1.3 WLAN 5 GHz Receiver Characteristics
		• Added TX power value for 802.11ax HE20 MCS9 in Section 5.12.1.4 WLAN 5 GHz Transmitter Characteristics
		• Updated Bluetooth LE maximum TX power in Section 5.12.2.2 Bluetooth LE Transmitter Characteristics
		• Added certain 802.15.4 RF characteristics values in Section 5.12.3.1 IEEE 802.15.4 Receiver Characteristics and 5.12.3.2 IEEE 802.15.4 Transmitter Characteristics

1.5	2025/7/24	• Changed the maximum MCU frequency in Section 1 Features • Corrected AUX ADC resolution in Section 1 Features and Section 2 Overview • Updated values for T_2, T_3, and T_4 in Table 4-2 Timing Parameters of Power-up Sequence in Section 4.6.1 Power Scheme • Updated the maximum baud rate of the UART interfaces in Section 4.11 UART Interfaces (UART) • Added I2C Fast-mode Plus feature in Section 4.13 I2C Interfaces (I2C) • Added description of dedicated hardware support for LED dimming/fading for the PWM module in Section 4.16 PWM Module (PWM) • Corrected the resolution, sampling rate range, and description of VBAT channel for the AUX ADC in Section 4.18 Auxiliary ADC (AUX ADC)

Version	Date	Description
		• Updated values of load capacitance and trim sensitivity for 40 MHz crystal in Section 5.9 40 MHz Crystal Characteristics • Added Section 5.10 32.768 kHz Crystal Characteristics • Updated AUX ADC Characteristics values in Section 5.13 AUX ADC Characteristics
1.6	2025/8/29	• Added 802.11ac support • Section 5.12 RF Characteristics: – Added a note regarding RF measurement conditions and the front-end circuit – Updated and added some characteristics values

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