# BK7236 Datasheet

DS-BK7236-E08 V1.6

2023/12/13

# Contents

# 1. Features

## Wi-Fi

- IEEE 802.11b/g/n/ax 1x1 compliant
- 20/40 MHz channel bandwidth for 2.4 GHz
- Supports downlink Multi-User Multiple-Input Multiple-Output (DL MU-MIMO)
- Supports Orthogonal Frequency Division Multiple Access (OFDMA)
- Supports Target Wake Time (TWT)
- TX and RX Low-Density Parity Check (LDPC) support for extended range
- WPA/WPA2/WPA3-Personal support for enhanced security
- Operating modes: STA, SoftAP, and Direct
- Concurrent AP + STA
- TX power up to +21 dBm
- RX sensitivity -98 dBm

## Bluetooth Low Energy

- Bluetooth 5.4 Low Energy (LE)
- Supports Bluetooth Low Energy 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Supported Bluetooth Low Energy features: LE audio, Angle of Arrival (AoA) and Angle of Departure (AoD) direction finding, 2 Mbps, advertising extensions, and long range
- Supports an antenna array with up to 16 antennas for precise positioning

## Core

- ARMv8-M Star (M33F) MCU at up to 320 MHz:
  - Double-precision floating-point unit (FPU)
  - 16 KB ITCM + 16 KB DTCM
  - Embedded TrustZone
  - Supports DSP instructions with SIMD
  - 3.84 CoreMark/MHz
- UART Flash download
- Serial Wire Debug (SWD) interface

## Memory

- SiP Flash: 4 MB or 8 MB
- SiP PSRAM: 4 MB or none
- 640 KB Share SRAM
- 64 KB ROM
- eFuse

## Security

The BK7236 integrates the IoT Platform Security Suite (IPSS) for cryptograph and system security control. The key features of the IPSS include:

- Secure boot
- Secure debug
- Secure connection
- Firmware Over-The-Air (FOTA)
- Provisioning
- TEE_M
- TrustEngine, which includes the following features:
  - Symmetric schemes, AES-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM (key size 128-bit, 192-bit and 256-bit)
  - Symmetric schemes, SM4-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM
  - Digest schemes, SHA1/224/256
  - Digest scheme, SM3
  - Asymmetric schemes, RSA 1024/2048/3072/4096 and ECCP 192/224/256/384/512/521
  - Asymmetric scheme, SM2
  - Key ladder for key management
  - Lifecycle management
  - True random number generator

## Clock Management

- External oscillator: 26 MHz crystal oscillator (XTALH), 32.768 kHz crystal oscillator (XTALL)
- Internal oscillator: 32 kHz ring oscillator (ROSC), 26–360 MHz digitally controlled oscillator (DCO)
- 320/480 MHz PLL (DPLL)
- Audio PLL (APLL)

## Power Management

- 2.0 to 5.5 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded buck (DC-DC) converters and LDO regulators
- Low power consumption:
  - Active mode RX: 17.5 mA
  - Sleep mode: 8 mA
  - Deep sleep mode: 17 µA
  - Shutdown mode: 2.5 µA

## Peripherals

- 21 GPIOs
- 1x SPI
- 3x UART: 1 with hardware flow control and Flash download support
- 1x SDIO
- 1x I2C
- 1x LIN controller
- 2x general-purpose DMA controller (GDMA), each with 12 channels
- 7x 32-bit PWM channel
- 12-bit AUX ADC, up to 7 channels
- 6x 32-bit general-purpose timer
- 2x watchdog timer (WDT)
- 1x real-time counter (RTC)
- 1x IrDA
- 1x temperature sensor
- 1x touch sensor, 6 touch sensing I/Os

## Packaging

- QFN40 package, 5 x 5 mm
- Operating temperature range: -40 up to +125 °C

## Applications

- Home appliance
  - Refrigerator

  - Air conditioner
  - Thermostat
  - Washing machine
  - Robot cleaner
- Smart plug
- Smart lighting
  - Light bulb
  - Light switch
  - Ceiling light
  - Stand light
- Others
  - Remote controller
  - Toy
  - Drone
  - Industrial terminal
  - Factory automation sensor/switch
  - Smart meter
  - Payment terminal
  - Industrial computer
  - Medical devices
  - Kitchen appliances
  - Home automation switch/sensor
  - Door lock
  - Door camera

# 2. Overview

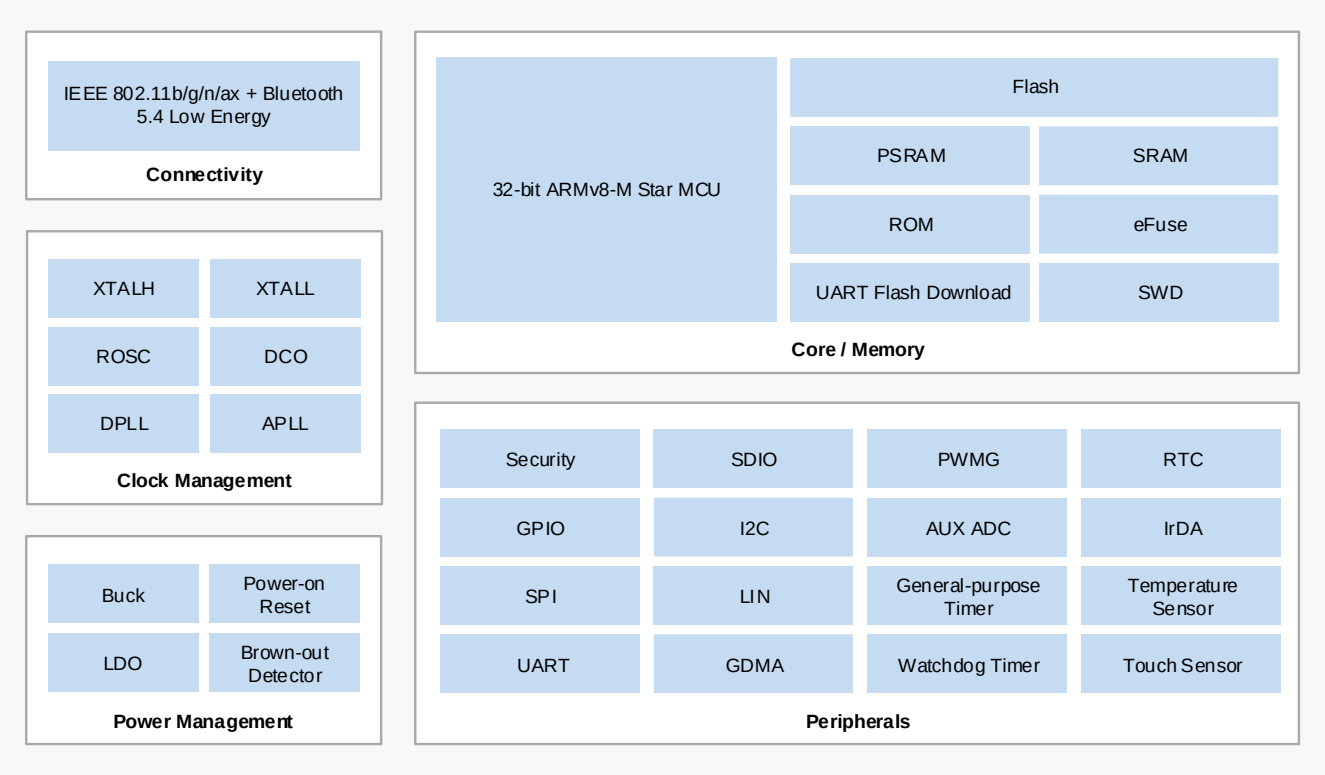
The BK7236 is a highly-integrated 1x1 single-band 2.4 GHz Wi-Fi 6 (802.11b/g/n/ax) and Bluetooth 5.4 Low Energy (LE) combo solution designed for applications that require high security and abundant resources. The integration of a 32-bit ARMv8-M Star MCU and a comprehensive set of peripherals makes the BK7236 ideal for advanced Internet of Things (IoT) applications.

The BK7236 provides state-of-the-art security based on a powerful security architecture. The BK7236 integrates a IoT Platform Security Suite (IPSS) for cryptograph and system security control. The IPSS embeds all-round and robust security features to set up a top-secret execution environment for IoT devices.

Using advanced design techniques and ultra-low power process technology, the BK7236 delivers high integration, efficient security and minimal power consumption for a wide range of advanced IoT applications.

Figure 2-1 shows the general block diagram of BK7236.

**Figure 2-1 BK7236 Block Diagram**



# 3. Pin Descriptions

The BK7236 provides Wi-Fi and Bluetooth LE functionality in a 5 x 5 mm, 40-pin QFN package.

## 3.1 QFN40 Pin Descriptions

Figure 3-1 shows the pin assignments of the QFN40 package.

**Figure 3-1 QFN40 Pin Assignments**

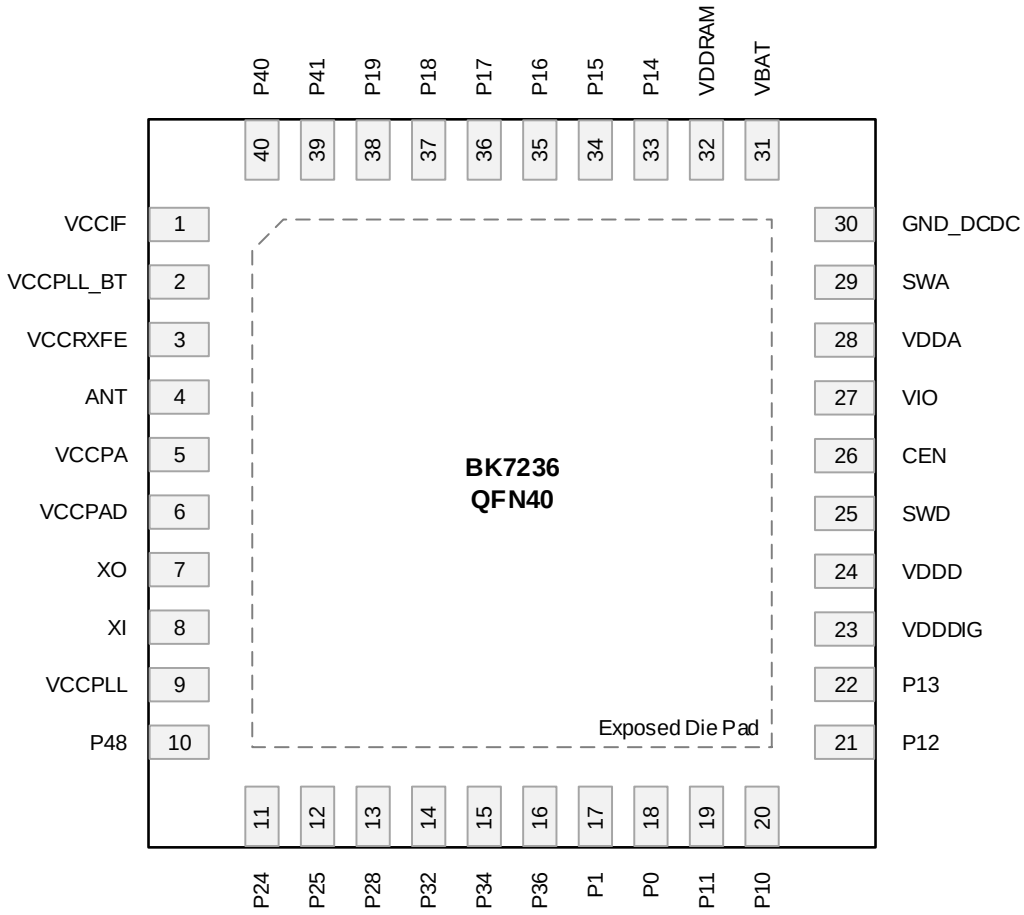



Table 3-1 shows the pin descriptions of the QFN40 package.

**Table 3-1 QFN40 Pin Descriptions**

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| 1 | VCCIF | - | Analog input | IF power supply |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| 2 | VCCPLL_BT | - | Analog input | Bluetooth RF PLL power supply |
| 3 | VCCRXFE | - | Analog input | RF receiver power supply |
| 4 | ANT | - | RF | 2.4 GHz RF signal port |
| 5 | VCCPA | - | Analog input | RF PA power supply |
| 6 | VCCPAD | - | Analog input | RF PA driver power supply |
| 7 | XO | - | Analog output | 26 MHz crystal output |
| 8 | XI | - | Analog input | 26 MHz crystal input |
| 9 | VCCPLL | - | Analog input | RF PLL power supply |
| 10 | P48 | I/O | Digital | GPIO48: general-purpose I/O |
| 11 | P24 | I/O | Digital/Analog | • GPIO24: general-purpose I/O<br>• LPO_CLK: 32 kHz clock output<br>• PWMG0_PWM4: PWMG0 channel PWM4<br>• ADC2: analog input channel |
| 12 | P25 | I/O | Digital/Analog | • GPIO25: general-purpose I/O<br>• IRDA: infrared data<br>• PWMG0_PWM5: PWMG0 channel PWM5<br>• ADC1: analog input channel |
| 13 | P28 | I/O | Digital/Analog | • GPIO28: general-purpose I/O<br>• I2S_MCLK: master clock<br>• ADC4: analog input channel<br>• TOUCH2: touch sensing I/O<br>• CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M) |
| 14 | P32 | I/O | Digital/Analog | • GPIO32: general-purpose I/O<br>• PWMG1_PWM0: PWMG1 channel PWM0<br>• TOUCH6: touch sensing I/O |
| 15 | P34 | I/O | Digital/Analog | • GPIO34: general-purpose I/O<br>• PWMG1_PWM2: PWMG1 channel PWM2<br>• TOUCH8: touch sensing I/O |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| | | | | • SPI0_CSN: chip select |
| 16 | P36 | I/O | Digital/Analog | • GPIO36: general-purpose I/O<br>• PWMG1_PWM4: PWMG1 channel PWM4<br>• TOUCH10: touch sensing I/O<br>• SPI0_MISO: master in slave out |
| 17 | P1 | I/O | Digital/Analog | • GPIO1: general-purpose I/O<br>• UART1_RX: receive data input<br>• I2C1_SDA: serial data<br>• SWDIO: serial wire data<br>• ADC13: analog input channel<br>• LIN_RXD: receive data input |
| 18 | P0 | I/O | Digital/Analog | • GPIO0: general-purpose I/O<br>• UART1_TX: transmit data output<br>• I2C1_SCL: serial clock<br>• SWCLK: serial wire clock<br>• ADC12: analog input channel<br>• LIN_TXD: transmit data output |
| 19 | P11 | I/O | Digital | • GPIO11: general-purpose I/O<br>• DL_UART_TX: UART Flash download transmit data output<br>• UART0_TX: transmit data output<br>• SDIO_DATA3: data |
| 20 | P10 | I/O | Digital | • GPIO10: general-purpose I/O<br>• DL_UART_RX: UART Flash download receive data input<br>• UART0_RX: receive data input<br>• SDIO_DATA2: data<br>• CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M) |
| 21 | P12 | I/O | Digital/Analog | • GPIO12: general-purpose I/O<br>• UART0_RTS: request to send<br>• TOUCH0: touch sensing I/O<br>• ADC14: analog input channel |
| 22 | P13 | I/O | Digital/Analog | • GPIO13: general-purpose I/O |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| | | | | • UART0_CTS: clear to send<br>• TOUCH1: touch sensing I/O<br>• ADC15: analog input channel |
| 23 | VDDDIG | - | Analog output | Digital core LDO output |
| 24 | VDDD | - | Analog output | Digital buck/LDO output |
| 25 | SWD | - | Analog output | Digital buck switch output |
| 26 | CEN | - | Analog input | Chip enable, active high |
| 27 | VIO | - | Analog output | IO LDO output |
| 28 | VDDA | - | Analog output | Analog buck/LDO output |
| 29 | SWA | - | Analog output | Analog buck switch output |
| 30 | GND_DCDC | - | GND | Buck ground |
| 31 | VBAT | - | Power | Chip power supply |
| 32 | VDDRAM | - | Analog output | PSRAM LDO output |
| 33 | P14 | I/O | Digital | • GPIO14: general-purpose I/O<br>• SDIO_CLK: clock<br>• SPI0_SCK: serial clock<br>• BT_ANT0: Bluetooth antenna select<br>• I2C1_SCL: serial clock |
| 34 | P15 | I/O | Digital | • GPIO15: general-purpose I/O<br>• SDIO_CMD: command/response<br>• SPI0_CSN: chip select<br>• BT_ANT1: Bluetooth antenna select<br>• I2C1_SDA: serial data |
| 35 | P16 | I/O | Digital | • GPIO16: general-purpose I/O<br>• SDIO_DATA0: data<br>• SPI0_MOSI: master out slave in<br>• BT_ANT2: Bluetooth antenna select |
| 36 | P17 | I/O | Digital | • GPIO17: general-purpose I/O<br>• SDIO_DATA1: data<br>• SPI0_MISO: master in slave out<br>• BT_ANT3: Bluetooth antenna select |
| 37 | P18 | I/O | Digital | • GPIO18: general-purpose I/O |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| | | | | • SDIO_DATA2: data<br>• PWMG0_PWM0: PWMG0 channel PWM0 |
| 38 | P19 | I/O | Digital/Analog | • GPIO19: general-purpose I/O<br>• SDIO_DATA3: data<br>• PWMG0_PWM1: PWMG0 channel PWM1 |
| 39 | P41 | I/O | Digital | • GPIO41: general-purpose I/O<br>• UART2_TX: transmit data output<br>• LIN_TXD: transmit data output |
| 40 | P40 | I/O | Digital | • GPIO40: general-purpose I/O<br>• UART2_RX: receive data input<br>• LIN_RXD: receive data input |
| Die pad | GND_SLUG | - | GND | Ground |

## 3.2 Pin Multiplexing

Table 3-2 shows the pin mux functions of GPIOs.

**Table 3-2 Pin Multiplexing**

| GPIO | Flash Download | Alternate Functions | | | | | |
|---|---|---|---|---|---|---|---|
| | | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 |
| | UART | UART1/UART0/ SDIO/Clock/ IrDA/UART2 | I2C1/SDIO/ SPI0/PWMG0/ Clock/PWMG1 | SWD/Clock/ ANT Select/ AUX ADC/LIN | TOUCH/I2C1 | AUX ADC/ Clock/SPI0 | LIN |
| GPIO0 | | UART1_TX | I2C1_SCL | SWCLK | | ADC12 | LIN_TXD |
| GPIO1 | | UART1_RX | I2C1_SDA | SWDIO | | ADC13 | LIN_RXD |
| GPIO10 | DL_UART_RX | UART0_RX | SDIO_DATA2 | CLK_AUXS_CIS | | | |
| GPIO11 | DL_UART_TX | UART0_TX | SDIO_DATA3 | | | | |
| GPIO12 | | UART0_RTS | | | TOUCH0 | ADC14 | |
| GPIO13 | | UART0_CTS | | | TOUCH1 | ADC15 | |
| GPIO14 | | SDIO_CLK | SPI0_SCK | BT_ANT0 | I2C1_SCL | | |
| GPIO15 | | SDIO_CMD | SPI0_CSN | BT_ANT1 | I2C1_SDA | | |
| GPIO16 | | SDIO_DATA0 | SPI0_MOSI | BT_ANT2 | | | |
| GPIO17 | | SDIO_DATA1 | SPI0_MISO | BT_ANT3 | | | |
| GPIO18 | | SDIO_DATA2 | PWMG0_PWM0 | | | | |
| GPIO19 | | SDIO_DATA3 | PWMG0_PWM1 | | | | |

| GPIO | Flash Download | Alternate Functions | | | | | |
|---|---|---|---|---|---|---|---|
| | | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 |
| | UART | UART1/UART0/ SDIO/Clock/ IrDA/UART2 | I2C1/SDIO/ SPI0/PWMG0/ Clock/PWMG1 | SWD/Clock/ ANT Select/ AUX ADC/LIN | TOUCH/I2C1 | AUX ADC/ Clock/SPI0 | LIN |
| GPIO24 | | LPO_CLK | PWMG0_PWM4 | ADC2 | | | |
| GPIO25 | | IRDA | PWMG0_PWM5 | ADC1 | | | |
| GPIO28 | | | I2S_MCLK | ADC4 | TOUCH2 | CLK_AUXS_CIS | |
| GPIO32 | | | PWMG1_PWM0 | | TOUCH6 | | |
| GPIO34 | | | PWMG1_PWM2 | | TOUCH8 | SPI0_CSN | |
| GPIO36 | | | PWMG1_PWM4 | | TOUCH10 | SPI0_MISO | |
| GPIO40 | | UART2_RX | | LIN_RXD | | | |
| GPIO41 | | UART2_TX | | LIN_TXD | | | |
| GPIO48 | | | | | | | |

# 4. Functional Description

## 4.1 Wi-Fi/Bluetooth Transceiver

The BK7236 integrates a high-performance Wi-Fi/Bluetooth transceiver. The incorporated low noise amplifier (LNA) amplifies the single-ended inputs and converts the amplified signals into differential outputs to achieve a better noise and linearity trade-off. On the transmit side, the differential outputs of the power amplifier (PA) are combined and converted to single-ended outputs using the on-chip balun, enabling transmit and receive operations with only one ANT pin connected to the antenna. The frequency synthesizer is fully integrated, eliminating the need for any external components.

## 4.2 Clock Management

The primary clock sources available in the BK7236 are as follows:

- High-frequency clocks
  - 26 MHz crystal oscillator: it outputs clock signal XTALH
  - 26–360 MHz internal digitally controlled oscillator (DCO): it outputs clock signal CLK_DCO
  - Digital PLL (DPLL): it generates 320 MHz clock CLK_320M and 480 MHz clock CLK_480M
- Low-frequency clocks
  - 32 kHz crystal oscillator: it outputs clock signal XTALL
  - 32 kHz internal ring oscillator (ROSC): it outputs clock signal CLK_ROSC
- Audio clock
  - Audio PLL (APLL): its default frequency is 98.304 MHz, and it outputs clock signal CLK_APLL

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32 kHz crystal oscillator XTALL
- 32 kHz clock signal derived from 26 MHz crystal oscillator
- 32 kHz internal oscillator ROSC

The BK7236 also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIOs can output the following clock signals:

- LPO_CLK: LPO_CLK clock
- I2S_MCLK: reference clock for external audio codec, derived from APLL

- CLK_AUXS_CIS: reference clock for external CMOS image sensor (CIS)

# 4.3 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown mode or deep sleep mode.

System power-on reset, digital power-on reset, and watchdog reset have the same reset effect on all blocks, except for the always-on logic. Any of these three resets can reset the whole chip to its initial state. The always-on logic has a 32-bit timer and 16-bit retention registers, which can only be reset to initial values by a system power-on reset.

Wake-up from either shutdown mode or deep sleep mode will power on digital from power-down mode, which triggers the whole system reset procedure.

# 4.4 Power Management

## 4.4.1 Power Scheme

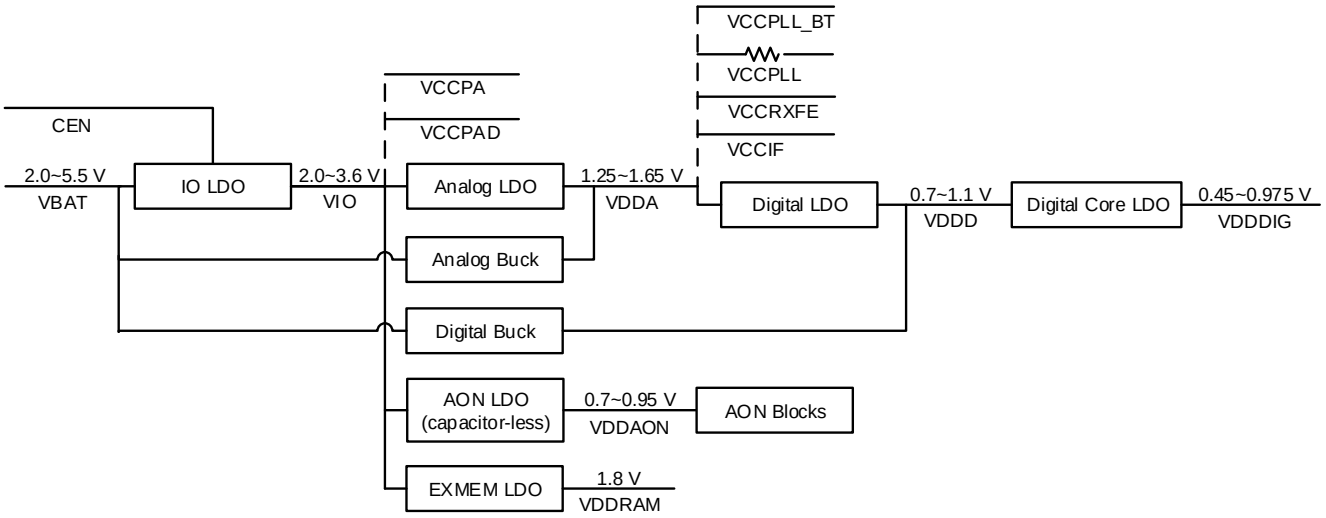
The power management system on the BK7236 includes two buck converters and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

The VBAT is the external main chip supply ranging from 2.0 to 5.5 V. The VBAT generates VIO through the IO LDO regulator. In addition to being the power supply for Wi-Fi PA, the VIO is also the input supply of analog LDO, AON LDO, and EXMEM LDO. The VBAT also generates VDDA and VDDD through the analog buck converter and the digital buck converter, respectively. The LDOs and bucks generate the following main power supplies:

- VDDA: power supply for RF/analog modules. It is externally connected to VCCPLL_BT/VCCPLL/VCCRXFE/ VCCIF to supply power to Wi-Fi/Bluetooth transceiver, and internally provides power supply to XTAL directly.
- VDDDIG: power supply for digital logic. It provides power supply for the processor, memory, Wi-Fi and Bluetooth baseband, as well as various peripherals.
- VDDAON: power supply for always-on (AON) logic. The AON logic, such as GPIOs, AON watchdog, RTC, and control logic of deep sleep wake-up, keeps working in deep sleep mode (VDDDIG off).
- VDDRAM: power supply for PSRAM.

Figure 4-1 shows the power distribution of BK7236.

**Figure 4-1 Internal Power Distribution**




**Note:** Outputs from the buck converters and LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the hardware schematic for details on selecting bypass capacitors.

Figure 4-2 shows the power-up sequence of BK7236.

**Figure 4-2 BK7236 Power-up Sequence**

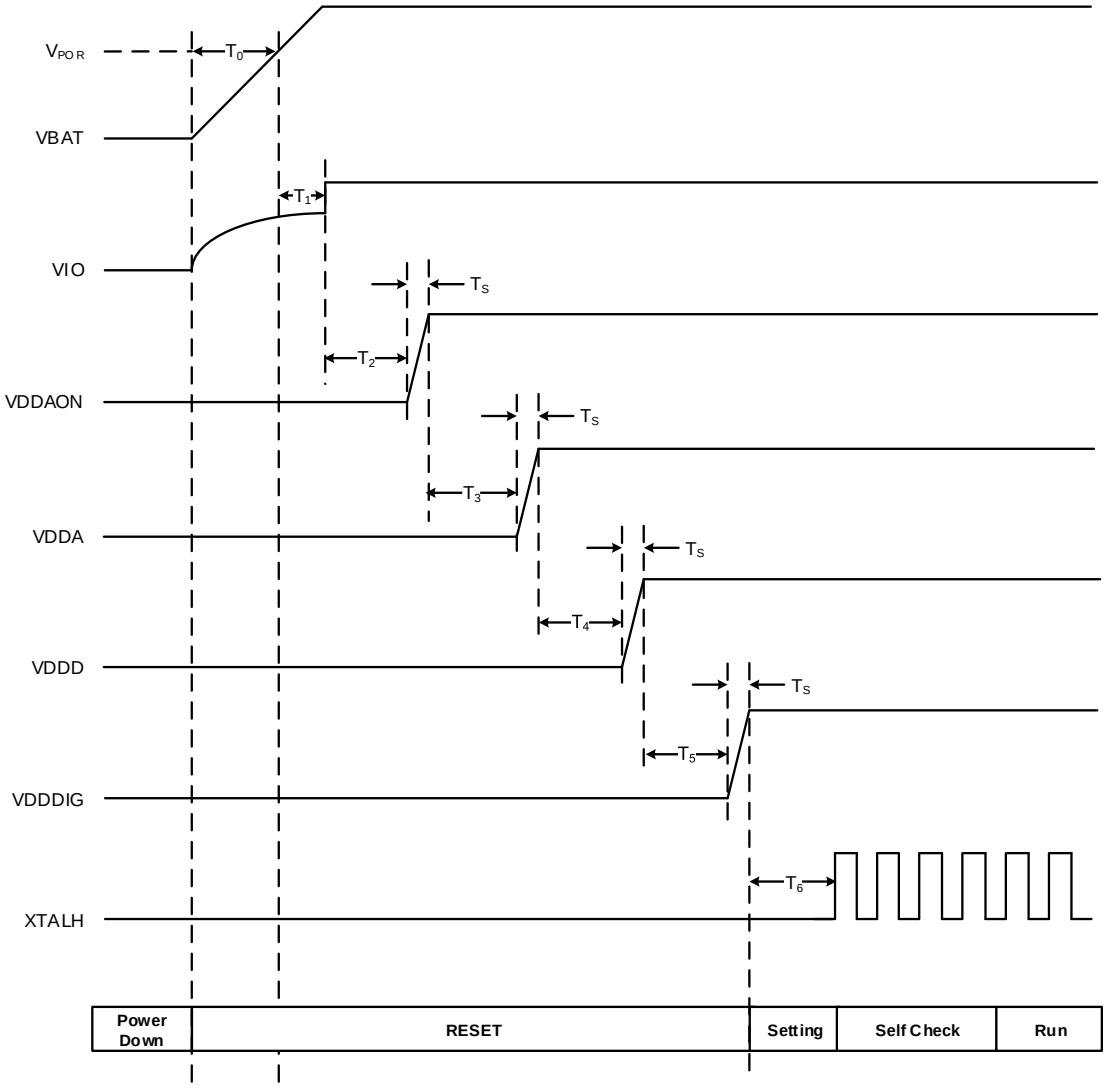



**Table 4-1 Timing Parameters of Power-up Sequence**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{POR}$ | VBAT POR threshold | - | 1.85 | - | V |
| $T_0$ | VBAT ready time | 200 | - | - | μs |
| $T_1$ | IO LDO output ready time | - | 240 | 500 | μs |
| $T_2$ | AON LDO output ready time | - | 240 | 500 | μs |
| $T_3$ | Analog buck/LDO output ready time | - | 240 | 500 | μs |

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_4$ | Digital buck/LDO output ready time | - | 240 | 500 | μs |
| $T_5$ | Digital core LDO output ready time | - | 240 | 500 | μs |
| $T_S$ | LDO settle time | 0 | - | - | μs |
| $T_6$ | XTALH stable time | - | 250 | 500 | μs |

### 4.4.2 Power Modes

The BK7236 supports three low-power modes except active mode, namely shutdown mode, deep sleep mode, and sleep mode, among which the shutdown mode has the lowest power consumption.

**Shutdown Mode:** All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

**Deep Sleep Mode:** All circuits are powered down except the AON logic. GPIO interrupts, RTC interrupts, or touch sensing I/O pins can power up the system again. Retention registers can keep their contents.

**Sleep Mode:** The MCU and all digital logic stop their clocks, and their power supply decreases to a much lower retention voltage, which results in a much lower current. GPIO interrupts, RTC interrupts, touch sensing I/O pins, or interrupts triggered by Wi-Fi/Bluetooth MAC low-power counters can bring the system back to active mode with normal voltage.

**Active Mode:** The MCU is active, and all peripherals are available.

## 4.5 General-purpose I/Os (GPIO)

The BK7236 has up to 21 GPIOs, which can be configured as either input or output. Most GPIOs are shared with alternate functions. Table 3-2 Pin Multiplexing provides the mux functions of GPIOs.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Interrupt generation:
  - High or low level
  - Rising or falling edge

## 4.6 SPI Interface (SPI)

The BK7236 integrates an SPI interface that can operate in master or slave mode. The SPI interface allows a clock frequency up to 40 MHz in both master and slave modes.

The SPI interface supports the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Embedded 64-depth RX FIFO and 64-depth TX FIFO with DMA capability

## 4.7 UART Interface (UART)

The BK7236 includes three Universal Asynchronous Receiver/Transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 2 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bit)
- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)
- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Hardware flow control with RTS and CTS signals (UART0)
- Flash download (UART0)
- Programmable digital filter

## 4.8 SDIO Interface (SDIO)

A secure digital input/output (SDIO) host/slave interface is available on the BK7236. It can be used as a host to read external SD cards or used by an external host as a slave to communicate with chips. The SDIO interface allows a maximum clock speed of 40 MHz.

The SDIO features include the following:

- SD memory card specification version 2.0 compliant
- SDIO card specification version 2.0 compliant

- Two data bus modes: 1-bit mode (default) and 4-bit mode
- Data transfer up to 40 Mbyte/s for the host mode and 20 Mbyte/s for the slave mode
- Supports DMA capability, allowing high-speed transfer without MCU load

## 4.9 I2C Interface (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7236 embeds an I2C interface, which can operate in master or slave mode.

The features of the I2C interface are listed below:

- Master and slave modes
- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection

## 4.10 LIN Controller (LIN)

The Local Interconnect Network (LIN) controller is a communication controller that performs serial communication. It implements the data link layer of the LIN Protocol Specification. The LIN protocol uses a single master/multiple slave concept for the frame transfer between nodes of the LIN network.

Features of the LIN controller are listed here:

- Support of LIN specification 2.2A
- Backward compatibility to LIN 1.3
- Configurable for support of master or slave functionality
- Programmable data rate between 1 kbit/s and 20 kbit/s (for master)
- Automatic bit rate detection (for slave)
- 8-byte data buffer
- 8-bit host controller interface

## 4.11 GDMA Controller (GDMA)

The BK7236 has two general-purpose DMA controllers (GDMA) with 12 DMA channels each to unload CPU activity. The 12 channels are shared by peripherals that have DMA capabilities.

The GDMA controllers can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). The GDMA controllers allow peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

The GDMA controllers support channel isolation. The DMA channels can be configured as secure/non-secure and as privileged/unprivileged channels:

- A non-secure channel performs non-secure DMA transfers
- A secure channel can perform secure or non-secure DMA transfers, with
  - Secure or non-secure data read from the source address
  - Secure or non-secure data write to the destination address
  - Via a TrustZone-aware DMA AHB master port
- An unprivileged channel performs unprivileged DMA transfers
- A privileged channel performs privileged DMA transfers

A selection of the peripherals on the BK7236 have DMA capabilities, including UART0, UART1, UART2, SPI0, SDIO, and AUX ADC.

## 4.12 PWM Group (PWMG)

The BK7236 has two advanced-control PWM groups (PWMG). Each PWMG consists of up to three independent 32-bit auto-reload counters driven by three programmable prescalers. The PWMGs can generate pulse width modulated signals for a variety of purposes, including input capture, pulse edge counting, or generation of output waveforms (output compare).

The features of one PWMG are listed here:

- Three 32-bit up, down, or up-and-down auto-reload counters
- Three 8-bit programmable prescalers capable of dividing the clock frequency of each counter by any factor between 1 and 256
- PWMG0 and PWMG1 both have three independent channels, among which:
  - PWM0/2/4
    - Input capture
    - Pulse edge counting
    - PWM generation (edge or center-aligned modes)
  - PWM1
    - Independent simple waveform generation (up-counting mode)
    - Coupled waveform (reverse or identical) generation when coupled with PWM0
- Channel PWM5 capable of generating coupled waveforms (reverse or identical) when coupled with PWM4

- Complementary outputs with programmable dead-time and configurable dead-time mode
- Synchronization circuit to control the counter with external signals and to interconnect several counters together
- Repetition counter to update the registers only after a given number of cycles of the counter
- Interrupt generation on the following events:
  - Update: counter overflow or underflow, counter initialization (by software or internal/external trigger)
  - Counter start
  - Input capture
  - Output compare
- Change of polarity, duty cycle, and base frequency on every PWM period
- Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes

Table 4-2 below provides the description of PWM signals.

**Table 4-2 PWM Signals**

| GPIO | PWM Pin Name | Signal Type | Description |
|---|---|---|---|
| **PWMG0** | | | |
| GPIO18 | PWMG0_PWM0 | I/O | PWMG0 channel PWM0 |
| GPIO19 | PWMG0_PWM1 | I/O | PWMG0 channel PWM1<br>PWM1 can work independently to generate simple waveforms or couple with PWM0 (with deadtime insertion) to generate reverse or identical waveforms of PWM0. |
| GPIO24 | PWMG0_PWM4 | I/O | PWMG0 channel PWM4 |
| GPIO25 | PWMG0_PWM5 | I/O | PWMG0 channel PWM5<br>PWM5 can couple with PWM4 (with deadtime insertion) to generate reverse or identical waveforms of PWM4. |
| **PWMG1** | | | |
| GPIO32 | PWMG1_PWM0 | I/O | PWMG1 channel PWM0 |
| GPIO34 | PWMG1_PWM2 | I/O | PWMG1 channel PWM2 |
| GPIO36 | PWMG1_PWM4 | I/O | PWMG1 channel PWM4 |

## 4.13 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 12-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot, software control, or continuous mode.

The AUX ADC module has the following features:

- Programmable sampling rate from 12.5 kHz to 650 kHz
- 12-bit resolution
- Up to 7 external analog input channels: ADC1/2/4/12/13/14/15
- Five internal dedicated channels:
  - VBAT monitoring channel (VBAT/2, VBAT/3, or VBAT/4), connected to ADC0
  - Internal temperature sensor (TEMP), connected to ADC7
  - TSSIO, connected to ADC8
  - Touch OUT_TD, connected to ADC9
  - Internal debug channel, connected to ADC11
- Conversion modes:
  - One-shot mode
  - Software control mode
  - Continuous mode

## 4.14 Timer Group (TIMG)

The BK7236 includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, factor between 1 and 16
- Capable of reading the real-time value of the counter

## 4.15 Watchdog Timers (WDT)

The BK7236 has two watchdog timers, the main domain watchdog timer (DWDT) and the always-on domain watchdog timer (AWDT). The purpose of the watchdog timers is to detect and recover from failures or malfunctions. The watchdog timers trigger a reset on expiry of a specified time period.

The DWDT runs on the 32 kHz LPO_CLK clock (factor 2/4/8/16) and has a maximum programmable period up to 32.768 (2^16/2 kHz) seconds. The AWDT runs on the ROSC and has a maximum programmable period up to 65.536 (2^16/1 kHz) seconds.

## 4.16 Real-Time Counter (RTC)

The real-time counter (RTC) module features a 64-bit counter and a tick event generator. The RTC runs on the 32 kHz LPO_CLK clock. It is used for low-power timing, and it can keep running even when the system is in deep sleep mode.

## 4.17 IrDA Interface (IrDA)

The BK7236 embeds a hardware IrDA interface to encode and decode signals. In addition, the interface has a capture timer capability that allows software decoding of the input signal.

The IrDA has the following features:

- Single-duplex mode
- Carrier modulation for transmission
- Integrated 512-byte RX FIFO and 512-byte TX FIFO

## 4.18 Temperature Sensor

The BK7236 integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results from the sensor can be read by the ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

## 4.19 Touch Sensor (TOUCH)

The BK7236 has six capacitive sensing I/Os, which immediately detect capacitance changes induced by touch or proximity of objects.

## 4.20 Security

The BK7236 provides state-of-the-art security based on a powerful security architecture. It integrates a total security solution for Internet of Things (IoT), IoT Platform Security Suite (IPSS). The IPSS aims to set up a top-secret execution environment for IoT devices. With the state-of-the-art security technology, it is intended for power/cost/resource sensitive IoT market applications.

The IPSS introduces a fundamental software IP solution for cryptograph and system security control. The key features of the IPSS include:

- Secure boot
- Secure debug
- Secure connection
- Firmware Over-The-Air (FOTA)
- Provisioning
- TEE_M
- TrustEngine

### System Architecture

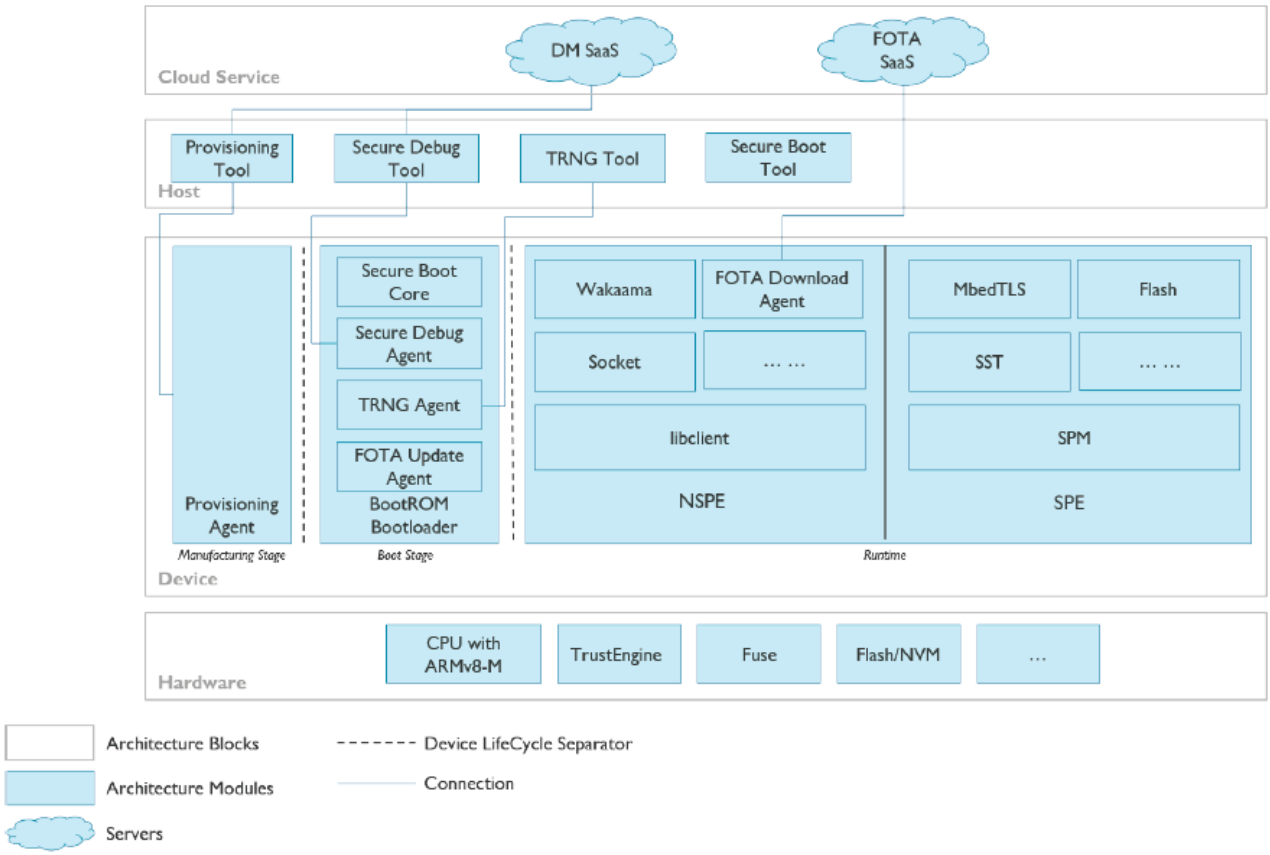
The IPSS software implements an all-round device-to-cloud security architecture, including:

- Provisioning mechanism in the manufacturing stage.
- Secure boot, secure debug, TRNG calibration, and FOTA update in the device boot stage.
- Secure connection and FOTA download in the device run-time stage.

IPSS also introduces a remote management solution to enable users to access, monitor and manage IoT devices in a secure manner. The remote management solution includes FOTA SaaS, Secure Debug SaaS, and Provisioning SaaS.

The following figure shows the architecture of the IPSS system.

**Figure 4-3 Security Architecture of the IPSS System**




## 4.20.1 Secure Boot

The secure boot solution provides the legitimacy and trustworthiness for images running on devices. It ensures that only official images which are published from OEMs are executable.

The secure boot functions include following aspects:

- Image verification
- Image encryption
- Extended program execution
- Image anti-rollback protection

## 4.20.2 Secure Debug

Secure debug provides a reliable mechanism for enabling the debug feature of a device after the device deployment.

Debug is one of the most commonly-used features in the device. With the debug feature, you can access all the device data, including the device firmware and the device root key.

### 4.20.3 FOTA

The FOTA solution implements a series of light-weight and trustworthy firmware upgrade interaction between IoT devices and servers, which includes downloading, verification, and installation.

### 4.20.4 Provisioning

Provisioning is the process to initialize secure credentials onto devices. It is required to happen in a secure environment such as the product line in the manufacturing stage.

The provisioning solution provides a full secure mechanism from the cloud server to devices. It keeps the security and integrity of provisioning materials, such as the device ID, model key, and the secure boot/secure debug public key hash, also keeps the device top secret such as the device root key that occurs only on the device side.

### 4.20.5 Secure Connection

The secure connection feature uses Mbed TLS to provide connection security in the transport layer over UDP. The key exchange method is Pre-Shared Key (PSK). The PSK's deployment happens in the manufacturing stage.

Mbed TLS provides cryptograph and SSL/TLS capabilities with TLS 1.1 and TLS 1.2.

### 4.20.6 BootROM

IPSS includes the BootROM reference code which is integrated with the secure boot solution.

There are primary boot and recovery boot paths in the BootROM.

- Primary boot is the main boot path. Normally devices should boot to the primary path.
- Recovery boot is the secondary boot path.

### 4.20.7 Bootloader

IPSS includes the Bootloader reference code which is integrated with the secure debug, provisioning, TRNG calibration, and FOTA solution.

In the primary bootloader, the secure debug agent, provisioning agent, and TRNG agent are integrated. The primary bootloader boots to the next image—TEE_M.

In the recovery bootloader, both the secure debug agent, TRNG agent, and the FOTA update agent are integrated. The recovery bootloader does not boot to any images.

### 4.20.8 TEE_M

IPSS introduces TEE_M. TEE_M provides an implementation of secure world software for ARMv8-M, which follows Arm Platform Security Architecture (PSA) PSA_Firmware_Framework_1.0-bet0. IPSS TEE_M provides the following services by default:

- Secure Storage: The Secure Storage (Only supports Protected Storage) service supports PSA_Storage_API-1.0-bet2 without extended functions.
- Crypto: The Crypto service supports PSA_Cryptography_API_Reference_1.0_bet1.
- DTLS: DTLS (leverages Mbed TLS) is integrated in TEE_M.

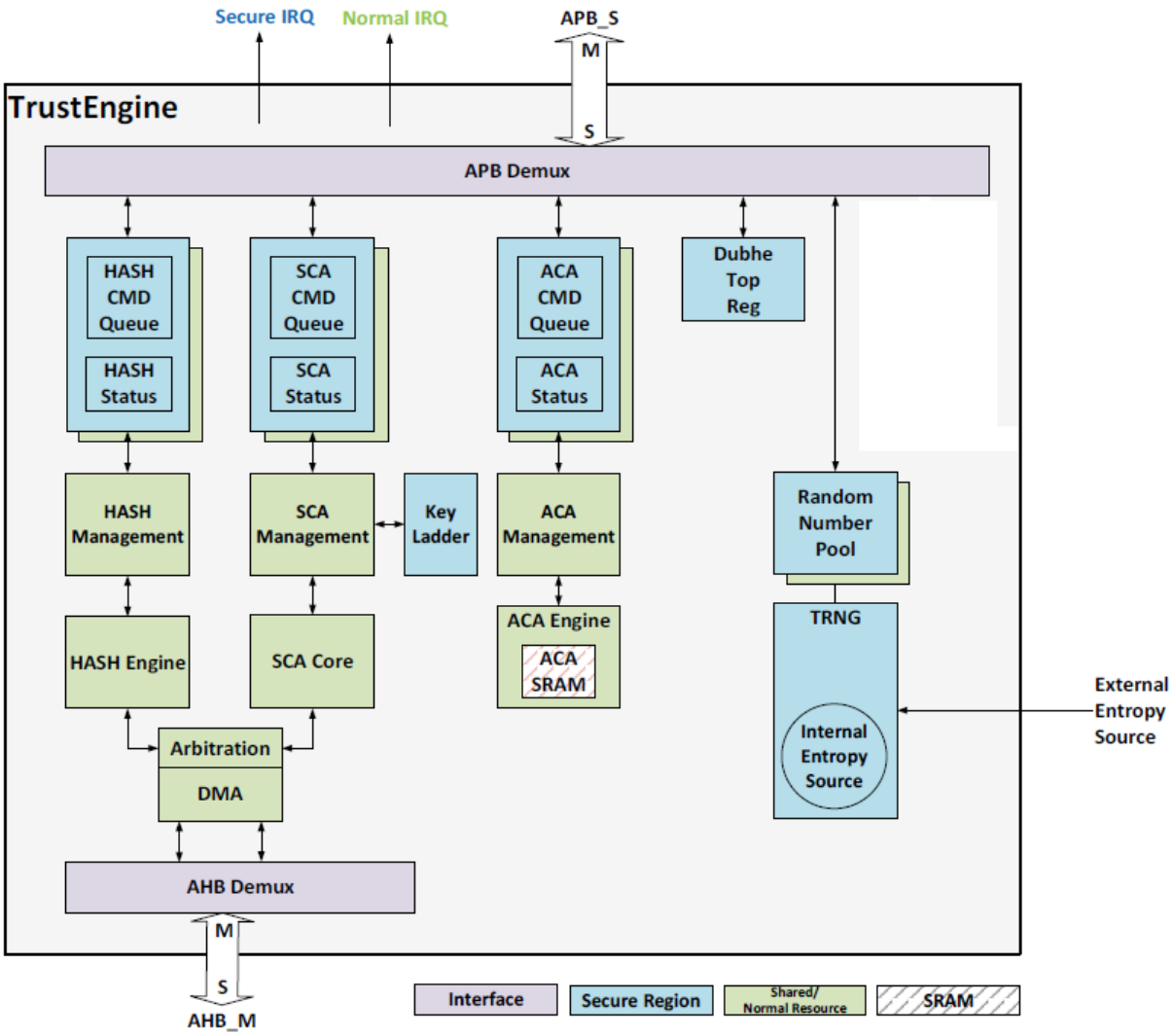
### 4.20.9 TrustEngine

IPSS introduces TrustEngine as a secure component in the system. It provides the following features:

- High security assurance. The crypto engine supports key ladders, lifecycle management and True Random Number Generator (TRNG) which enhance the system security.
- High performance and low power for encryption/decryption operation. This is achieved by TrustEngine internal cryptography engines.
- Reduction of software complicity in security. Some security functions are implemented in TrustEngine hardware, which can reduce the risk of sensitive information leakage to non-secure hosts.

The following figure shows the TrustEngine top-level architecture.

**Figure 4-4 TrustEngine Top-Level Architecture**




### 4.20.9.1 Features

TrustEngine includes the following features:

- Symmetric schemes, AES-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM (key size 128-bit, 192-bit and 256-bit)
- Symmetric schemes, SM4-ECB/CBC/CTR/CBC-MAC/CMAC/CCM/GCM
- Digest schemes, SHA1/224/256
- Digest scheme, SM3
- Asymmetric schemes, RSA 1024/2048/3072/4096 and ECCP 192/224/256/384/512/521
- Asymmetric scheme, SM2
- Key ladder for key management

- Lifecycle management
- True random number generator

#### 4.20.9.2 Supported Standards and Specifications

TrustEngine is compliant with the following standards:

- FIPS PUB 180-4: Secure Hash Standard (SHS)
- FIPS PUB 197: Advanced Encryption Standard (AES)
- NIST SP 800-38A Recommendation for Block Cipher Modes of Operation-Methods and Techniques
- NIST SP 800-38B Recommendation for Block Cipher Modes of Operation: The CMAC Mode for Authentication
- NIST SP 800-38C Recommendation for Block Cipher Modes of Operation-the CCM Mode for Authentication and Confidentiality
- NIST SP 800-38D, Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC
- NIST SP 800-90B Recommendation for the Entropy Sources Used for Random Bit Generation
- SM2 Public Key Cryptographic Algorithm Based on Elliptic Curves (GB/T 32918-2016)
- SM3 Cryptographic Hash Algorithm (GB/T 32905-2016)
- SM4 Block Cipher Algorithm (GB/T 32907-2016)

#### 4.20.9.3 Components

TrustEngine consists of five major function blocks.

- Symmetric Cryptography Accelerator (SCA)
- Asymmetric Cryptography Accelerator (ACA)
- HASH engine
- One-time programmable storage access controller
- True random number generator

##### Symmetric Cryptography Accelerator (SCA)

SCA in TrustEngine is responsible for data encryption/decryption using the symmetric cryptography algorithm. The data encryption/decryption operations are performed through the SCA engine by sending special commands to TrustEngine.

##### Asymmetric Cryptography Accelerator (ACA)

The ACA engine in TrustEngine is responsible for accelerating the asymmetric cryptography, such as:

- Asymmetric encryption and decryption: RSA and ECC
- Digital signature and verification: RSA signatures and ECDSA
- Key exchange: DH (Diffie-Hellman) and ECDH

## HASH Accelerator

The HASH engine in TrustEngine is responsible for digest calculation. The digest of certain data can be calculated through the HASH engine by sending special commands to TrustEngine.

## True Random Number Generator

The True Random Number Generator (TRNG) generates the random bits using the internal entropy source (ring oscillator inverter chain) or the external entropy source. The random bits are required by both secure and non-secure hosts.

# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| VBAT | Battery regulator supply voltage | -0.3 | 5.5 | V |
| VIO | IO LDO output voltage | -0.3 | 3.6 | V |
| VCCPA | Supply voltage for PA | -0.3 | 3.6 | V |
| VCCPAD | Supply voltage for PA driver | -0.3 | 3.6 | V |
| VCCIF | Supply voltage for IF | -0.3 | 1.65 | V |
| VCCRXFE | Supply voltage for RX | -0.3 | 1.65 | V |
| VCCPLL | Supply voltage for RF PLL | -0.3 | 1.65 | V |
| VCCPLL_BT | Supply voltage for Bluetooth RF PLL | -0.3 | 1.65 | V |
| VDDA | Analog LDO output voltage | -0.3 | 1.65 | V |
| VDDD | Digital LDO output voltage | -0.3 | 1.1 | V |
| VDDDIG | Digital core LDO output voltage | -0.3 | 0.975 | V |
| VDDRAM | PSRAM LDO output voltage | -0.3 | 3.6 | V |
| SWA | Analog buck switch output voltage | -0.3 | 5.5 | V |
| SWD | Digital buck switch output voltage | -0.3 | 5.5 | V |
| $P_{RX}$ | RX input power | - | 10 | dBm |
| $T_{STR}$ | Storage temperature range | -55 | 150 | ℃ |

## 5.2 ESD Ratings

| Parameter | Description | Test Condition | Value | Unit |
|---|---|---|---|---|
| ESD HBM | Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001-2017 | - | TBD | V |

| Parameter | Description | Test Condition | Value | Unit |
|---|---|---|---|---|
| ESD CDM | Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002-2018 | - | TBD | V |

## 5.3 Recommended Operating Conditions

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VBAT | Battery regulator supply voltage | 2.0 | - | 5.5 | V |
| VIO | IO LDO output voltage | 2.0 | - | 3.6 | V |
| VCCPA | Supply voltage for PA | 2.0 | - | 3.6 | V |
| VCCPAD | Supply voltage for PA driver | 2.0 | - | 3.6 | V |
| VCCIF | Supply voltage for IF | 1.25 | - | 1.65 | V |
| VCCRXFE | Supply voltage for RX | 1.25 | - | 1.65 | V |
| VCCPLL | Supply voltage for RF PLL | 1.25 | - | 1.65 | V |
| VCCPLL_BT | Supply voltage for Bluetooth RF PLL | 1.25 | - | 1.65 | V |
| VDDA | Analog LDO output voltage | 1.25 | - | 1.65 | V |
| VDDD | Digital LDO output voltage | 0.7 | - | 1.1 | V |
| VDDDIG | Digital core LDO output voltage | 0.45 | - | 0.975 | V |
| VDDRAM | PSRAM LDO output voltage | - | 1.8 | - | V |
| VBAT slew rate | - | 300 | - | - | mV/ms |
| $T_{OPR}$ | Operating temperature range | -40 | - | 125 | ℃ |

## 5.4 Digital I/O Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VIH | High-level input voltage | - | 0.7 VIO | - | VIO + 0.3 | V |
| VIL | Low-level input voltage | - | -0.3 | - | 0.3 VIO | V |
| VOH | High-level output voltage | - | 0.9 VIO | - | - | V |
| VOL | Low-level output voltage | - | - | - | 0.1 VIO | V |
| $I_{DRV}$ | I/O output drive strength | - | 5 | - | 20 | mA |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Weak pull-up resistor | - | - | 40 | - | kΩ |
| $R_{PD}$ | Weak pull-down resistor | - | - | 44 | - | kΩ |

## 5.5 Analog Buck

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDDA | Buck/LDO output voltage | 1.25 | 1.4 | 1.65 | V |
| Load current | - | - | - | 150 | mA |
| Switching frequency | Buck modulation frequency | 0.5 | 1 | 2 | MHz |
| Output filter capacitor capacitance | - | - | 4.7 | - | μF |
| Inductor inductance | - | - | 4.7 | - | μH |
| Inductor DC resistance | - | - | - | 500 | mΩ |
| Inductor saturation current | - | 300 | - | - | mA |

## 5.6 Digital Buck

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDDD | Buck/LDO output voltage | 0.75 | 1.05 | 1.1 | V |
| Load current | - | - | - | 100 | mA |
| Switching frequency | Buck modulation frequency | 0.5 | 1 | 2 | MHz |
| Output filter capacitor capacitance | - | - | 4.7 | - | μF |
| Inductor inductance | - | - | 4.7 | - | μH |
| Inductor DC resistance | - | - | - | 500 | mΩ |
| Inductor saturation current | - | 200 | - | - | mA |

## 5.7 Analog LDO

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDDA | Analog LDO output voltage | 1.15 | 1.35 | 1.5 | V |
| Load current | - | - | - | 150 | mA |

## 5.8 Digital LDO

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDDD | Digital LDO output voltage | 0.7 | 1.0 | 1.05 | V |
| Load current | - | - | - | 100 | mA |

## 5.9 Core LDO

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDDDIG | Digital core LDO output voltage | 0.45 | 0.9 | 0.975 | V |
| Load current | - | - | - | 100 | mA |

## 5.10 26 MHz Crystal Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| F0 | Nominal Frequency | - | - | 26 | - | MHz |
| ΔF/F0 | Frequency tolerance | 25 ℃ | -10 | - | +10 | ppm |
| TC | Frequency stability over operating temperature | -40 to 105 ℃ crystal | -20 | - | +20 | ppm |
| | | -30 to 85 ℃ crystal | -10 | - | +10 | ppm |
| CL | Load capacitance | - | 7 | 7.3 | 9 | pF |
| TS | Trim sensitivity | -40 to 105 ℃ crystal | - | 32 | - | ppm/pF |
| | | -30 to 85 ℃ crystal | - | 17 | - | ppm/pF |

## 5.11 Current Consumption

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Active Mode** | | | | | |
| RX current | 11b: 11 Mbps DSSS | - | 17.5 | - | mA |
| | 11g: 54 Mbps OFDM | - | 17.5 | - | mA |
| | 11n: MCS7, HT20 | - | 17.5 | - | mA |
| | 11n: MCS7, HT40 | - | TBD | - | mA |
| | 11ax: MCS7, HE20 | - | 17.5 | - | mA |
| TX current | 11b: 11 Mbps DSSS @ 17 dBm | - | 249 | - | mA |
| | 11g: 54 Mbps OFDM @ 15 dBm | - | 215 | - | mA |
| | 11n: MCS7, HT20 @ 14 dBm | - | 216 | - | mA |
| | 11n: MCS7, HT40 @ 14 dBm | - | TBD | - | mA |
| | 11ax: MCS7, HE20 @ 14 dBm | - | TBD | - | mA |
| **Sleep Mode** | | | | | |
| Sleep | - | - | 8 | - | mA |
| Deep sleep | - | - | 17 | - | µA |
| **Shutdown Mode** | | | | | |
| Shutdown | - | - | 2.5 | - | µA |

## 5.12 WLAN RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Frequency range | - | 2412 | - | 2484 | MHz |
| **Sensitivity** | | | | | |
| Sensitivity - IEEE 802.11b | 1 Mbps DSSS | - | -98 | - | dBm |

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| (8% PER for 1024 octet PSDU) | 2 Mbps DSSS | - | -94.5 | - | dBm |
| | 5.5 Mbps DSSS | - | -92 | - | dBm |
| | 11 Mbps DSSS | - | -89 | - | dBm |
| Sensitivity - IEEE 802.11g (10% PER for 1000 octet PSDU) | 6 Mbps OFDM | - | -92 | - | dBm |
| | 9 Mbps OFDM | - | -91.5 | - | dBm |
| | 12 Mbps OFDM | - | -90.5 | - | dBm |
| | 18 Mbps OFDM | - | -88 | - | dBm |
| | 24 Mbps OFDM | - | -85 | - | dBm |
| | 36 Mbps OFDM | - | -82 | - | dBm |
| | 48 Mbps OFDM | - | -77.5 | - | dBm |
| | 54 Mbps OFDM | - | -76.5 | - | dBm |
| Sensitivity - IEEE 802.11n, 20 MHz (10% PER for 4096 octet PSDU, LDPC) | HT20, MCS0 | - | -92 | - | dBm |
| | HT20, MCS1 | - | -91 | - | dBm |
| | HT20, MCS2 | - | -88 | - | dBm |
| | HT20, MCS3 | - | -86 | - | dBm |
| | HT20, MCS4 | - | -82 | - | dBm |
| | HT20, MCS5 | - | -78 | - | dBm |
| | HT20, MCS6 | - | -76.5 | - | dBm |
| | HT20, MCS7 | - | -75 | - | dBm |
| Sensitivity - IEEE 802.11n, 40 MHz (10% PER for 4096 octet PSDU, LDPC) | HT40, MCS0 | - | -87.5 | - | dBm |
| | HT40, MCS1 | - | -87 | - | dBm |
| | HT40, MCS2 | - | -85 | - | dBm |
| | HT40, MCS3 | - | -82.5 | - | dBm |
| | HT40, MCS4 | - | -79 | - | dBm |
| | HT40, MCS5 | - | -75 | - | dBm |
| | HT40, MCS6 | - | -74 | - | dBm |
| | HT40, MCS7 | - | -71.5 | - | dBm |
| Sensitivity - IEEE 802.11ax, 20 MHz | HE20, MCS0 | - | -92 | - | dBm |

| Parameter | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| (10% PER for 4096 octet PSDU, LDPC) | HE20, MCS1 | | - | -90.5 | - | dBm |
| | HE20, MCS2 | | - | -87.5 | - | dBm |
| | HE20, MCS3 | | - | -85 | - | dBm |
| | HE20, MCS4 | | - | -81 | - | dBm |
| | HE20, MCS5 | | - | -77.5 | - | dBm |
| | HE20, MCS6 | | - | -75.5 | - | dBm |
| | HE20, MCS7 | | - | -74 | - | dBm |
| Sensitivity - IEEE 802.11ax, 40 MHz<br>(10% PER for 4096 octet PSDU, LDPC) | HE40, MCS0 | | - | -88.5 | - | dBm |
| | HE40, MCS1 | | - | -87.5 | - | dBm |
| | HE40, MCS2 | | - | -85.5 | - | dBm |
| | HE40, MCS3 | | - | -82 | - | dBm |
| | HE40, MCS4 | | - | -77 | - | dBm |
| | HE40, MCS5 | | - | -75 | - | dBm |
| | HE40, MCS6 | | - | -74 | - | dBm |
| | HE40, MCS7 | | - | -72 | - | dBm |
| **Maximum Receive Level** | | | | | | |
| Maximum receive level @ 2.4 GHz | 11b: 1, 2 Mbps (8% PER, 1024 octets) | | - | 10 | - | dBm |
| | 11b: 5.5, 11 Mbps (8% PER, 1024 octets) | | - | 10 | - | dBm |
| | 11g: 6–54 Mbps (10% PER, 1000 octets) | | - | 0 | - | dBm |
| | 11n: MCS0–7 (10% PER, 4096 octets) | | - | 0 | - | dBm |
| | 11ax: MCS0–7 (10% PER, 4096 octets) | | - | 0 | - | dBm |
| **Adjacent Channel Rejection** | | | | | | |
| Adjacent channel (±30 MHz) rejection - IEEE 802.11b<br>(8% PER for 1024 octet PSDU with desired signal level as specified in Condition) | 1 Mbps DSSS | -74 dBm | - | 50 | - | dB |
| | 2 Mbps DSSS | -74 dBm | - | 45 | - | dB |

| Parameter | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Adjacent channel (±25 MHz) rejection - IEEE 802.11b<br>(8% PER for 1024 octet PSDU with desired signal level as specified in Condition) | 5.5 Mbps DSSS | -70 dBm | - | 43 | - | dB |
| | 11 Mbps DSSS | -70 dBm | - | 40 | - | dB |
| Adjacent channel (±25 MHz) rejection - IEEE 802.11g<br>(10% PER for 1000 octet PSDU with desired signal level as specified in Condition) | 6 Mbps OFDM | -79 dBm | - | 43 | - | dB |
| | 54 Mbps OFDM | -62 dBm | - | 27 | - | dB |
| Adjacent channel (±25 MHz) rejection - IEEE 802.11n<br>(10% PER for 4096 octet PSDU with desired signal level as specified in Condition) | HT20, MCS0 | -79 dBm | - | 43 | - | dB |
| | HT20, MCS7 | -61 dBm | - | 21 | - | dB |
| Adjacent channel (±40 MHz) rejection - IEEE 802.11n<br>(10% PER for 4096 octet PSDU with desired signal level as specified in Condition) | HT40, MCS0 | -76 dBm | - | TBD | - | dB |
| | HT40, MCS7 | -58 dBm | - | TBD | - | dB |
| Adjacent channel (±20 MHz) rejection - IEEE 802.11ax<br>(10% PER for 4096 octet PSDU with desired signal level as specified in Condition) | HE20, MCS0 | -79 dBm | - | 43 | - | dB |
| | HE20, MCS7 | -61 dBm | - | 26 | - | dB |
| Adjacent channel (±40 MHz) rejection - IEEE 802.11ax<br>(10% PER for 4096 octet PSDU with desired signal level as specified in Condition) | HE40, MCS0 | -76 dBm | - | TBD | - | dB |
| | HE40, MCS7 | -58 dBm | - | TBD | - | dB |
| **Spurious Emissions** | | | | | | |
| Spurious emissions | < 1 GHz | | - | -60 | - | dBm |
| | > 1 GHz | | - | -50 | - | dBm |

## 5.13 WLAN RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Frequency range | - | 2412 | - | 2484 | MHz |
| **TX power** | | | | | |
| TX power - IEEE 802.11b (SEM compliant) | 1 Mbps DSSS | - | 21 | - | dBm |
| | 11 Mbps DSSS | - | 21 | - | dBm |
| TX power - IEEE 802.11g (EVM compliant) | 6 Mbps OFDM | - | 18 | - | dBm |
| | 54 Mbps OFDM | - | 18 | - | dBm |
| TX power - IEEE 802.11n (EVM compliant) | HT20, MCS0 | - | 17 | - | dBm |
| | HT20, MCS7 | - | 17 | - | dBm |
| | HT40, MCS0 | - | 17 | - | dBm |
| | HT40, MCS7 | - | 16 | - | dBm |
| TX power - IEEE 802.11ax (EVM compliant) | HE20, MCS0 | - | 17 | - | dBm |
| | HE20, MCS7 | - | 17 | - | dBm |
| | HE40, MCS0 | - | 17 | - | dBm |
| | HE40, MCS7 | - | 16 | - | dBm |
| **Spurious Emissions** | | | | | |
| Spurious emissions (at maximum output power) | < 1 GHz | - | -50 | - | dBm |
| | > 1 GHz | - | -45 | - | dBm |

## 5.14 Bluetooth LE RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Frequency range | - | 2402 | - | 2480 | MHz |

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Bluetooth LE 1 Mbps** | | | | | |
| Sensitivity | 30.8% PER | - | -97 | - | dBm |
| Maximum input level | 30.8% PER | - | 0 | - | dBm |
| C/I co-channel | - | - | 8 | - | dB |
| C/I 1 MHz adjacent channel | - | - | 0 | - | dB |
| C/I -1 MHz adjacent channel | - | - | 0 | - | dB |
| C/I 2 MHz adjacent channel | - | - | -26 | - | dB |
| C/I -2 MHz adjacent channel | - | - | -27 | - | dB |
| C/I 3 MHz adjacent channel | - | - | -28 | - | dB |
| C/I -3 MHz adjacent channel | - | - | -29 | - | dB |
| C/I > 3 MHz adjacent channel | - | - | -50 | - | dB |
| C/I < -3 MHz adjacent channel | - | - | -50 | - | dB |
| Out-of-band blocking | 30–2000 MHz | -10 | - | - | dBm |
| | 2003–2399 MHz | -12 | - | - | dBm |
| | 2484–2997 MHz | -12 | - | - | dBm |
| | 3000 MHz–12.75 GHz | -2 | - | - | dBm |
| Intermodulation | - | - | TBD | - | dBm |
| **Bluetooth LE 2 Mbps** | | | | | |
| Sensitivity | 30.8% PER | - | -94 | - | dBm |
| Maximum input level | 30.8% PER | - | 0 | - | dBm |
| C/I co-channel | - | - | 7 | - | dB |
| C/I 2 MHz adjacent channel | - | - | 0 | - | dB |
| C/I -2 MHz adjacent channel | - | - | 3 | - | dB |
| C/I 4 MHz adjacent channel | - | - | -26 | - | dB |
| C/I -4 MHz adjacent channel | - | - | -30 | - | dB |
| C/I 6 MHz adjacent channel | - | - | -30 | - | dB |
| C/I -6 MHz adjacent channel | - | - | -39 | - | dB |
| C/I > 6 MHz adjacent channel | - | - | -22 | - | dB |

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| C/I < -6 MHz adjacent channel | - | - | -22 | - | dB |
| Out-of-band blocking | 30–2000 MHz | - | -30 | - | dBm |
| | 2003–2399 MHz | - | -35 | - | dBm |
| | 2484–2997 MHz | - | -35 | - | dBm |
| | 3000 MHz–12.75 GHz | - | -17 | - | dBm |
| Intermodulation | - | - | TBD | - | dBm |
| **Bluetooth LE 125 kbps** | | | | | |
| Sensitivity | 30.8% PER | - | -102 | - | dBm |
| Maximum input level | 30.8% PER | - | 0 | - | dBm |
| C/I co-channel | - | - | 3 | - | dB |
| C/I 1 MHz adjacent channel | - | - | -15 | - | dB |
| C/I -1 MHz adjacent channel | - | - | -16 | - | dB |
| C/I 2 MHz adjacent channel | - | - | -34 | - | dB |
| C/I -2 MHz adjacent channel | - | - | -40 | - | dB |
| C/I 3 MHz adjacent channel | - | - | -42 | - | dB |
| C/I -3 MHz adjacent channel | - | - | -43 | - | dB |
| C/I > 3 MHz adjacent channel | - | - | -41 | - | dB |
| C/I < -3 MHz adjacent channel | - | - | -42 | - | dB |
| **Bluetooth LE 500 kbps** | | | | | |
| Sensitivity | 30.8% PER | - | -99 | - | dBm |
| Maximum input level | 30.8% PER | - | 0 | - | dBm |
| C/I co-channel | - | - | 5 | - | dB |
| C/I 1 MHz adjacent channel | - | - | -2 | - | dB |
| C/I -1 MHz adjacent channel | - | - | -3 | - | dB |
| C/I 2 MHz adjacent channel | - | - | -30 | - | dB |
| C/I -2 MHz adjacent channel | - | - | -31 | - | dB |
| C/I 3 MHz adjacent channel | - | - | -31 | - | dB |
| C/I -3 MHz adjacent channel | - | - | -40 | - | dB |

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| C/I > 3 MHz adjacent channel | - | - | -36 | - | dB |
| C/I < -3 MHz adjacent channel | - | - | -36 | - | dB |

## 5.15 Bluetooth LE RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| Frequency range | | - | 2402 | - | 2480 | MHz |
| TX power | | - | -20 | 6 | 15 | dBm |
| **Bluetooth LE 1 Mbps** | | | | | | |
| In-band emissions | ±2 MHz offset | - | - | -47 | - | dBm |
| | ±3 MHz offset | - | - | -49 | - | dBm |
| | >±3 MHz offset | - | - | -50 | - | dBm |
| Modulation characteristics | Δf1avg | - | 225 | 245 | 275 | kHz |
| | Δf2max | - | 185 | 235 | - | kHz |
| | Δf2avg/Δf1avg | - | 0.8 | 0.93 | - | - |
| Carrier frequency offset and drift | Max $\|f_n\|$ n = 0, 1, 2, 3…k | - | - | 3 | 150 | kHz |
| | Max $\|f_0 - f_n\|$ n = 2, 3, 4…k | - | - | 2.5 | 50 | kHz |
| | $\|f_1 - f_0\|$ | - | - | 2 | 23 | kHz |
| | Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k | - | - | 2.5 | 20 | kHz/50 µs |
| **Bluetooth LE 2 Mbps** | | | | | | |
| In-band emissions | ±4 MHz offset | - | - | -50 | - | dBm |
| | ±5 MHz offset | - | - | -51 | - | dBm |
| | >±5 MHz offset | - | - | -52 | - | dBm |
| Modulation characteristics | Δf1avg | - | - | 488 | - | kHz |
| | Δf2max | - | - | 469 | - | kHz |
| | Δf2avg/Δf1avg | - | - | 0.93 | - | - |

| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Carrier frequency offset and drift | Max $\|f_n\|$ n = 0, 1, 2, 3…k | - | - | 3 | 150 | kHz |
| | Max $\|f_0 - f_n\|$ n = 2, 3, 4…k | - | - | 2.5 | 50 | kHz |
| | $\|f_1 - f_0\|$ | - | - | 1.5 | 23 | kHz |
| | Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k | - | - | 2.5 | 20 | kHz/50 µs |
| **Bluetooth LE 125 kbps** | | | | | | |
| In-band emissions | ±2 MHz offset | - | - | -47 | - | dBm |
| | ±3 MHz offset | - | - | -49 | - | dBm |
| | >±3 MHz offset | - | - | -50 | - | dBm |
| Modulation characteristics | Δf1avg | - | 225 | 245 | 275 | kHz |
| | Δf1max | - | 185 | 246 | - | kHz |
| Carrier frequency offset and drift | Max $\|f_n\|$ n = 0, 1, 2, 3…k | - | - | 1.5 | 150 | kHz |
| | Max $\|f_0 - f_n\|$ n = 1, 2, 3…k | - | - | 1.5 | 50 | kHz |
| | $\|f_0 - f_3\|$ | - | - | 1.5 | 19.2 | kHz |
| | $\|f_n - f_{n-3}\|$ n = 7, 8, 9…k | - | - | 1.5 | 19.2 | kHz/48 µs |
| **Bluetooth LE 500 kbps** | | | | | | |
| In-band emissions | ±2 MHz offset | - | - | -47 | - | dBm |
| | ±3 MHz offset | - | - | -49 | - | dBm |
| | >±3 MHz offset | - | - | -50 | - | dBm |

## 5.16 AUX ADC Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Conversion clock | - | - | - | 13 | MHz |
| Conversion time | - | - | 16 | - | Cycle |
| $V_{REF}$ | Internal | - | 1.2 | - | V |
| | External | - | VIO/2 | - | V |
| Input voltage range | - | 0 | - | VREF*2 | V |

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input impedance | - | 10 | - | - | MΩ |
| Input capacitance (Cs) | - | - | 1 | - | pF |
| DNL | - | -1 | - | 3 | LSB |
| INL | - | -5 | - | 5 | LSB |
| ENOB | - | - | 10 | - | Bit |
| SNDR | - | - | 62 | - | dB |
| SFDR | - | - | 77 | - | dB |
| $T_{STARTUP}$ | - | - | 5 | - | μs |
| Current consumption | - | - | 200 | - | μA |

# 6. Package Information

**Figure 6-1 QFN40 5 x 5 mm Package Outline**

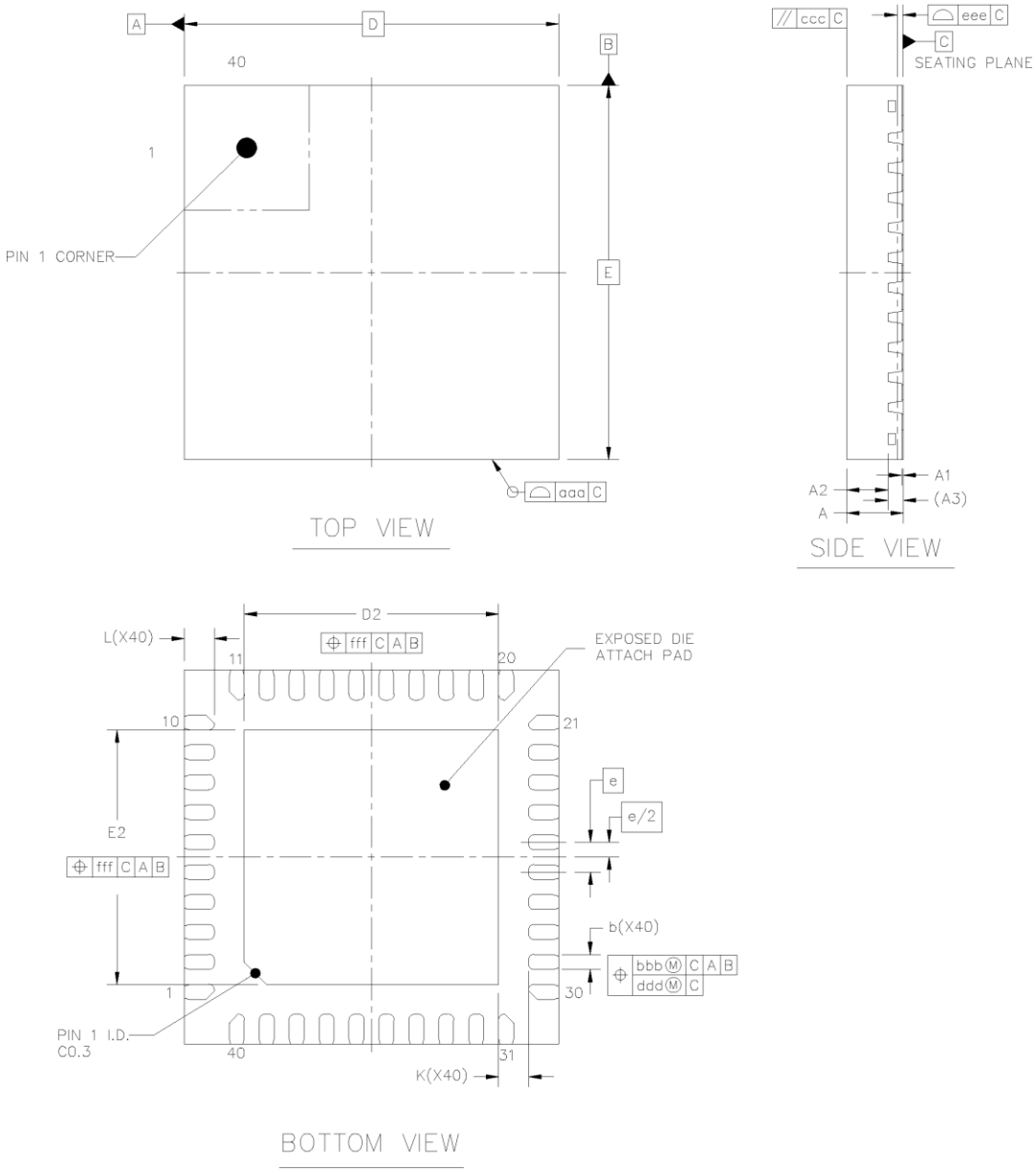
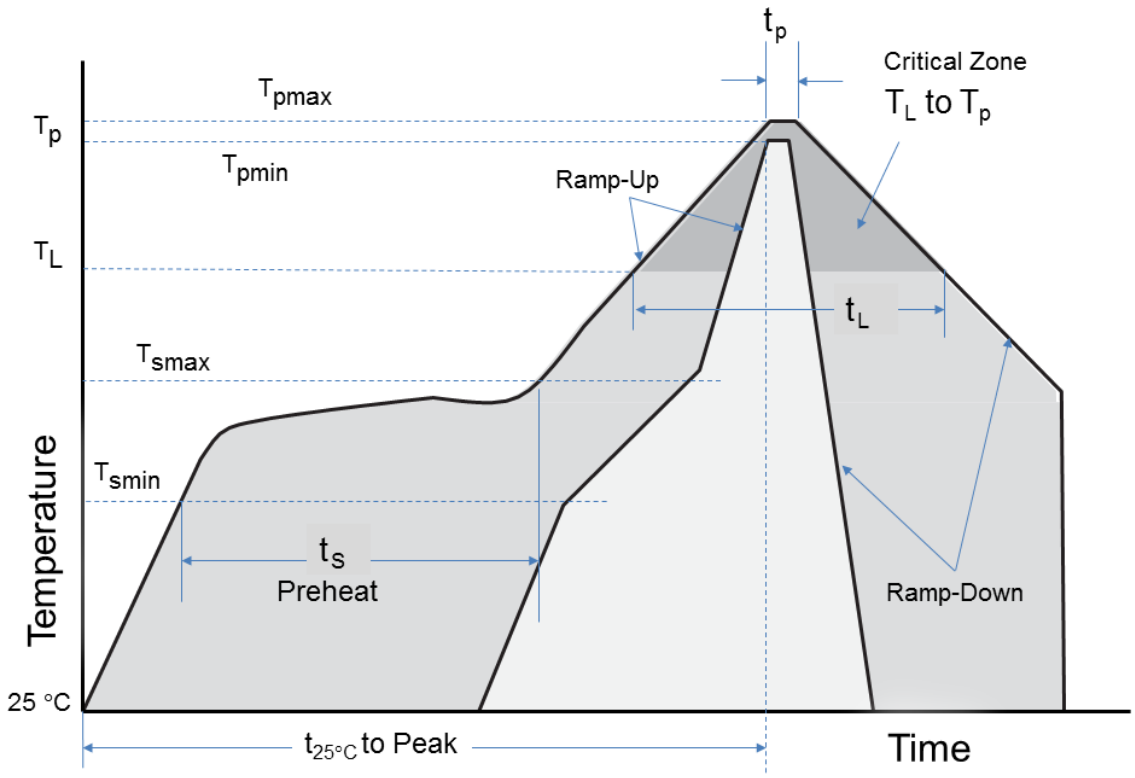


**Table 6-1 QFN40 Package Dimensions**

| Symbol | Dimensions in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | - | 0.55 | - |
| A3 | 0.203 REF | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 5.00 BSC | | |
| E | 5.00 BSC | | |
| e | 0.40 BSC | | |
| D2 | 3.30 | 3.40 | 3.50 |
| E2 | 3.30 | 3.40 | 3.50 |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.40 REF | | |
| aaa | 0.10 | | |
| ccc | 0.10 | | |
| eee | 0.08 | | |
| bbb | 0.07 | | |
| ddd | 0.05 | | |
| fff | 0.10 | | |

# 7. Reflow Soldering Profile

**Figure 7-1 Reflow Soldering Profile**




| Profile Feature | | Specification |
|---|---|---|
| Average ramp-up rate ($T_{smax}$ to $T_p$) | | 3 ℃/s max. |
| Preheat | Temperature min. ($T_{smin}$) | 150 ℃ |
| | Temperature max. ($T_{smax}$) | 200 ℃ |
| | Time ($t_s$) | 60 s to 180 s |
| Time maintained above | Temperature ($T_L$) | 217 ℃ |
| | Time ($t_L$) | 60 s to 150 s |
| Peak/classification temperature ($T_p$) | | 260 ℃ |
| Time within 5 ℃ of actual peak temperature ($t_p$) | | 20 s to 40 s |

| Profile Feature | Specification |
|---|---|
| Ramp-down rate | 6 ℃/s max. |
| Time 25 ℃ to peak temperature | 8 minutes max. |

## RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, or DIBP content in accordance with EU RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU.

## ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

## Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

# 8. Ordering Information

**Figure 8-1 Part Number Scheme**

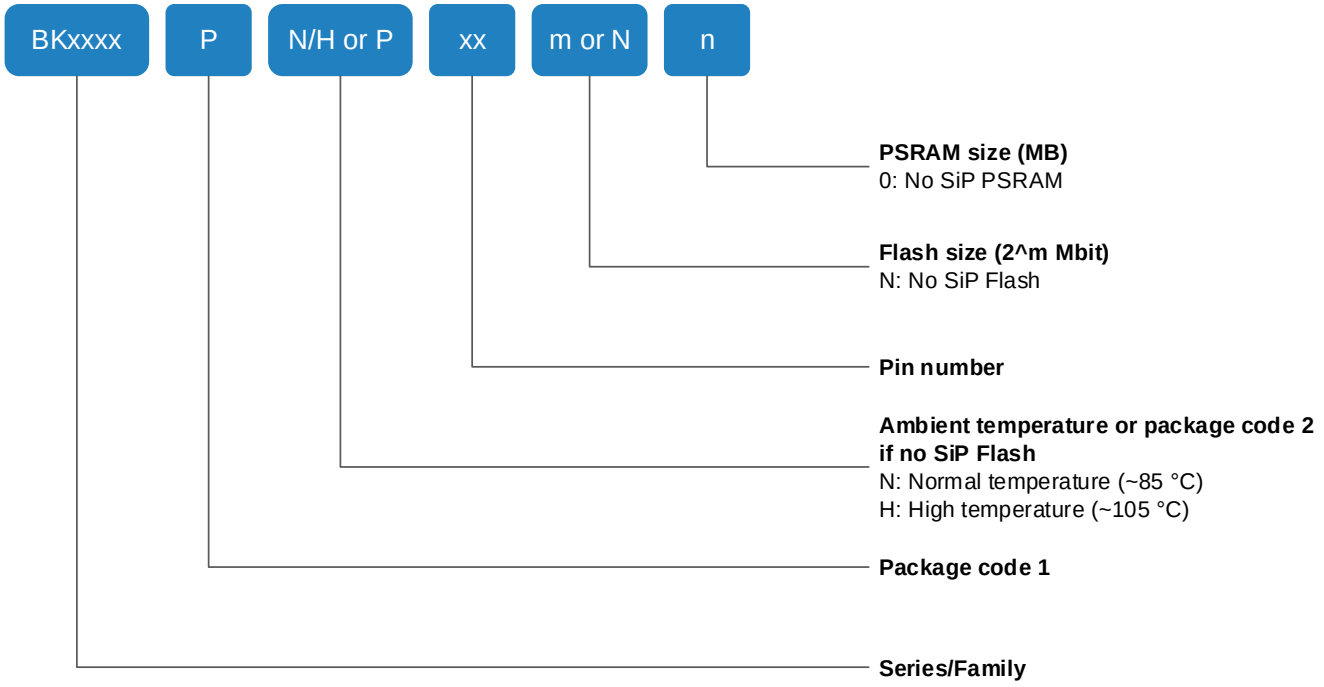



**Table 8-1 Ordering Information**

| Ordering Code | Package | SiP[a] Flash | SiP PSRAM | Packing | Minimum Ordering Qty (MOQ) |
|---|---|---|---|---|---|
| BK7236QN4050 | 5 mm x 5 mm QFN40 | 4 MB | - | Tape and Reel | 3000 |

a. A system in a package (SiP) refers to Flash/PSRAM enclosed in the package.

# Revision History

| Version | Date | Description |
|---|---|---|
| 0.1 | 2022/7/8 | Initial release |
| 1.0 | 2022/12/14 | Updated the pin assignments for pin 39 and pin 40 in Section 3 Pin Descriptions |
| 1.1 | 2023/3/2 | • General wording fixes<br>• Updated TX power in Section 1 Features<br>• Updated compliance with Bluetooth Specification to Bluetooth 5.4 in Section 1 Features and Section 2 Overview<br>• Updated core frequency in subsection Core of Section 1 Features<br>• Removed JTAG from, added SPI flash download and SWD interface to subsection Core of Section 1 Features<br>• Removed cache from subsection Memory of Section 1 Features<br>• Updated full-speed USB to high-speed USB in Section 1 Features<br>• Updated the number of GDMA controllers and GDMA channel number in Section 1 Features and Section 4.11 GDMA Controller (GDMA)<br>• Updated the number of PWM in Section 1 Features<br>• Updated the resolution of SAR ADC in Section 1 Features and Section 4.13 Auxiliary ADC (AUX ADC)<br>• Updated Figure 2-1 BK7236 Block Diagram in Section 2 Overview<br>• Updated pin assignments of the QFN40 package and GPIO mapping of PWM in Section 3 Pin Descriptions<br>• Corrected the description of clock signals can be output by GPIOs in Section 4.2 Clock Management<br>• Updated SPI frequency in Section 4.6 SPI Interface (SPI)<br>• Updated the original Section USB<br>• Updated Section 4.12 PWM Group (PWMG)<br>• Updated Section 4.14 Timer Group (TIMG)<br>• Updated Section 4.15 Watchdog Timers (WDT)<br>• Updated Section 4.16 Real-Time Counter (RTC)<br>• Add parameter VDDRAM to Section 5.1 Absolute Maximum Ratings and Section 5.3 Recommended Operating Conditions<br>• Updated storage temperature range in Section 5.1 Absolute Maximum Ratings<br>• Removed Section BUCKPA from Section 5 Electrical Characteristics<br>• Updated WLAN TX power in Section 5.13 WLAN RF Transmitter Characteristics |

| Version | Date | Description |
|---|---|---|
| | | • Updated SAR ADC characteristics values in Section 5.16 AUX ADC Characteristics |
| 1.2 | 2023/3/31 | Removed 802.11ac support |
| 1.3 | 2023/6/9 | • Renamed some interfaces and peripherals<br>• Updated Section 1 Features<br>• Updated Section 2 Overview<br>• Updated pin assignments and pin description for QFN40 package in Section 3 Pin Descriptions<br>• Updated Section 4 Functional Description<br>• Updated and added measurement data in Section 5 Electrical Characteristics<br>• Added Section 5.2 ESD Ratings and Section 5.4 Digital I/O Characteristics |
| 1.4 | 2023/6/16 | • Updated dual-mode Bluetooth support to Bluetooth Low Energy support<br>• Updated core description |
| 1.5 | 2023/9/25 | • General wording fixes<br>• Updated OFDMA and TWT support and added Bluetooth LE features in Section 1 Features<br>• Renamed low-voltage sleep mode to sleep mode and removed normal sleep mode throughout document<br>• Updated pin assignments for QFN40 package<br>• Corrected pin assignments for UART0 CTS and RTS in Section 3 Pin Descriptions<br>• Updated Section 4.2 Clock Management<br>• Added FIFO feature for IrDA interface in Section 4.17 IrDA Interface (IrDA)<br>• Corrected absolute max. ratings for VDDD and VDDDIG in Section 5.1 Absolute Maximum Ratings<br>• Updated ordering information in Section 8 Ordering Information |
| 1.6 | 2023/12/13 | • Updated QFN40 pin assignments: updated the number of I2C interfaces, PWM channels, ADC channels, and touch sensing I/Os, and removed DISPLAY controller and CLK26M clock signal<br>• Updated Wi-Fi RX sensitivity, and updated and added current values in Section 1 Features<br>• Updated Section 3 Pin Descriptions<br>• Updated the note on selecting bypass capacitors in Section 4.4.1 Power Scheme<br>• Updated the description of PWM channels in Section 4.12 PWM Group (PWMG) |

| Version | Date | Description |
|---|---|---|
| | | • Removed note “Values currently listed in this section are preliminary measurements and are subject to change.” from Section 5 Electrical Characteristics<br>• Added VBAT slew rate to Section 5.3 Recommended Operating Conditions<br>• Updated and added current values in Section 5.11 Current Consumption<br>• Updated and added RF characteristic values in Section 5.12 WLAN RF Receiver Characteristics to Section 5.15 Bluetooth LE RF Transmitter Characteristics<br>• Updated QFN40 package outline and mechanical specifications in Section 6 Package Information<br>• Updated RoHS compliance statement in Section 7 Reflow Soldering Profile |

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